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Despite the above, we will be making copies of essential technical information (circuit diagram, parts list, layout) freely available to all via our website as time and effort permit. This will be done to try and encourage and enable the maintenance of our remaining stock of vintage electronic equipment.

Guidance on using this electronic document

Opening the file

You need to view this document with Acrobat Reader **version 5.0** or later (current version at time of writing is v8). This software is available free of charge from Adobe. It is also widely distributed with many other software and hardware products. You can upgrade your Acrobat Reader by direct download from the internet at http://www.adobe.com/products/reader/ - or going to http://www.adobe.com/ and navigating from there.

It is possible that the document may open with a version of the Acrobat Reader earlier than 5.0 (thus allowing you to get this far!), but is also likely that some pages will not be shown correctly.

Reading the file on-screen

When you open the file, you will see the first page displayed, and also a list of headings down the left hand side. These are "bookmarks", which provide you with an "on-screen index". By (left) clicking on any of these headings, you will be taken immediately to the page it refers to. This enables quick navigation around the document.

Large diagrams

The large diagrams (larger than A4) are given in two formats – in A4 size "sub-sheets" to allow easy printing, and also as A3 complete sheets. When you click on a bookmark for a large diagram, you are taken to the A3 version, so you can see the whole diagram on-screen. When you print the document, the A4 versions of these pages are used. (You can of course print the A3 size sheets, if you are lucky enough to have an A3 format printer).

Printing the document

The document started life on paper, and one aim of these archive copies is to provide a good record of the original. If you want to, you can make a pretty accurate copy of the original from our file.

The vast majority of our users have access only to an A4 format printer (this is the common paper size available in UK and Europe, which measures 29.7cm by 21.0cm), and special steps have been taken to provide accurate reproduction of large pages (typically A3 size or large).

To keep close to the original, our file is intended for double-sided printing – that is printing on both sides of one sheet of paper. Nearly all original documents are printed in this way to keep their size to a minimum and save paper. This also means that you will occasionally get a blank sheet – because the original had exactly that. It also means that properly bound copies will remain readable – no text disappearing into the binding if the copy is properly paginated.

Large sheets are a problem if you have only an A4 format printer. Shrinking such sheets to half size (or smaller) is not generally an answer because they often become unreadable without a magnifying glass. The solution used here is for you to print A3 sheets as two overlapping A4 sheets (overlap size is 1.5cm), and then cut and paste them together.

A4 double-sided printing

Double-sided printers (automatic) are becoming increasingly common, however double-siding can often be achieved manually by first printing the odd sides only, then turning the sheets over, feeding them through again and printing the even sides. Your printer manual will explain how to do this for your specific printer (don't assume its dead straightforward – read the manual!).

The following instructions are based on Adobe Reader v8, and other versions may differ in detail:

1. Work out the page numbers you want to print. If you want to print the whole document, then within "Bookmarks" (see "*Reading the file on-screen"* above), first click on "**Front….**", and note the page number given at the bottom of the Acrobat window – this will give you the page number of the first page to be printed. Similarly click on "**End of A4 printable copy**", to determine the last page to be printed. (If you are only printing part of the document, then just note the page range you want.)
2. Select "File – Print" or click on the printer icon. This will bring up the print dialog box.
3. Select the correct printer if necessary.
4. In the area marked "Print Range" click on the radio button marked "Pages from..", then enter the first and last page numbers worked out in step 1 into the "from" and "to" boxes.

5. If your printer has automatic double-siding, you may still need to select “double-sided printing” if this not an option you use by default.
6. If you are using manual double-siding, then change the “subset” setting from “All pages in range” to “Odd pages only”.
7. In the “Page Handling” area, next to “Page Scaling”, select “Fit to paper”. The press “OK”

If you are doing manual double-siding, then you will need to repeat steps 2 to 7, but in step 6, substitute “Even pages only” for “Odd pages only”. You will need to refer to your printer manual to understand exactly how to feed the sheets back through the printer (which way round to place them) – or find out how to do this by trial and error.

A4 single-sided printing

Single-sided printing is straightforward. You will just use more paper! And you will get the occasional blank sheet, which you can remove from the stack of printed pages, and re-use in your printer. Just follow the instructions under double-sided printing but ignore all references to double-siding.

Printing the document on an US Letter format printer

Since A4 and US Letter sizes are similar, it is expected that this document should print satisfactorily on the latter format paper. This has not been tested however, and is not guaranteed. Follow the steps as for A4 printing, and make doubly sure that “Fit to paper” is selected (step 7).

Any other problems?

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Richard Hankins, January 2008

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RECEIVER, RADIO, R234

TECHNICAL HANDBOOK - TECHNICAL DESCRIPTION

This EMER must be read in conjunction with Tels E 612 Part 2 which contains figures and tables to which reference is made.

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RECEIVER, RADIO, R234

Introduction

1. The Receiver, Radio, R234 is a high frequency double superheterodyne communications receiver covering the frequency band 2.1-27Mc/s. It provides facilities for reception of the following types of transmission:-

Double sideband telephony (d.s.b.)	A3
Single sideband telephony (s.s.b.)	A3a
Independent sideband telephony (i.s.b.)	A3b
C.W. telegraphy (c.w.)	A1
Frequency shift keyed telegraphy (f.s.k.)	F1

2. The receiver is used in mobile role in Stations, radio, D11/R234 and in Stations, radio, D13/R234 (2 dual diversity), and in static role in Stations, radio, D13/R234 (2 dual diversity), static.

3. Fig 1 is a block diagram of the D11/R234 station. The Adaptor antenna receiver or the Transformer r.f. antenna coupling matches the various station antennae to the 75Ω co-axial input of the receiver.

4. Simplex or duplex operation is possible. When working simplex the antenna change-over system and desensitizing circuits prevent overloading of the receiver input circuit by the signal from the adjacent transmitter.

5. When operating duplex with the transmitter and receiver working simultaneously on different frequencies using separate antennae, the acceptor unit protects the receiver input circuit from damage and prevents blocking and cross-modulation taking place.

6. Power for the station is provided by a 3.5kVA trailer mounted generating set.

7. Rapid frequency selection with high resetting accuracy is made possible by the inclusion in the receiver of a crystal calibrator and an unconventional decade switching system combined with a normal tuning system.

8. Receiver sensitivity depends upon the mode and frequency of operation. Generally, an input of 1.5-2.5μV is sufficient for a 20dB signal/noise ratio on telegraphy, s.s.b. and i.s.b. reception. When working d.s.b. the sensitivity is approximately halved.

BRIEF DESCRIPTION

Construction

9. The receiver is made up of five units which are housed in a robust aluminium cabinet fitted with shock absorbent mountings.

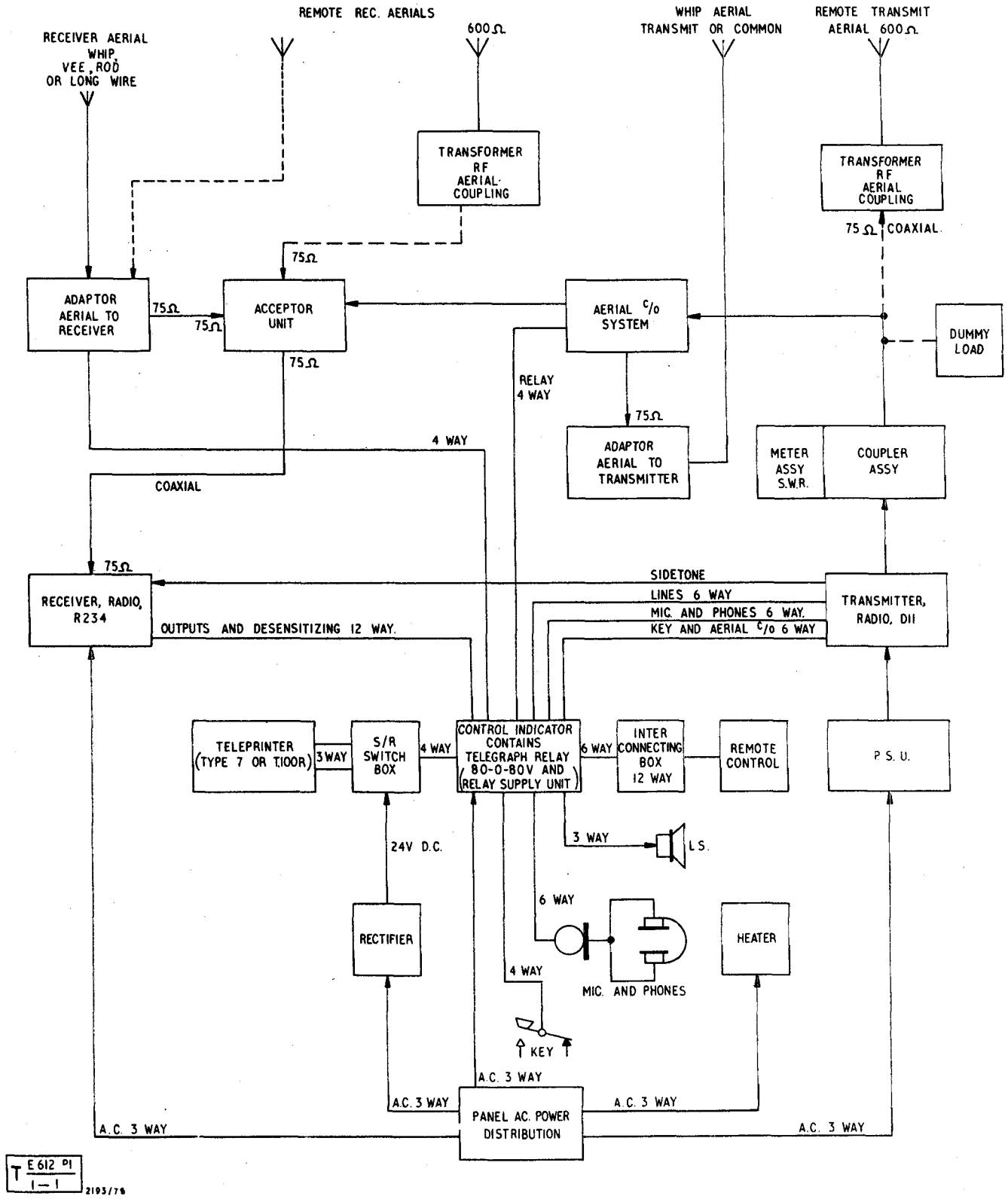

Fig 1 - Station,Radio, D11/R234, block diagram

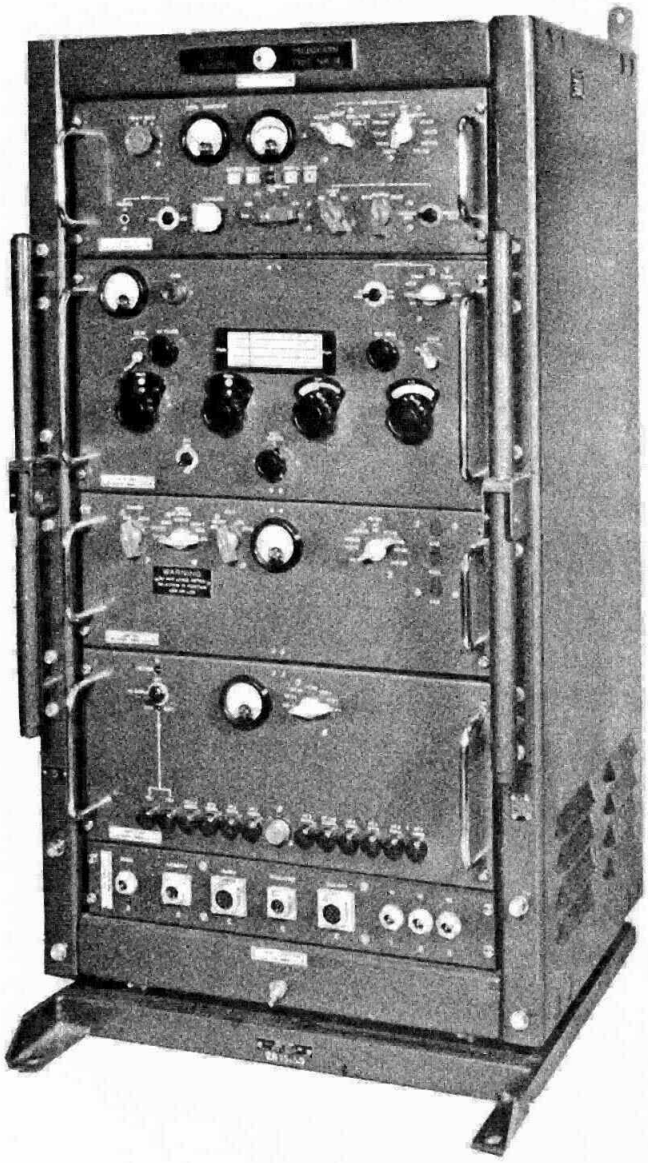

Fig 2 - Receiver, Radio, R234, general view

10. The telegraph, s.s.b. and power supply units are constructed on heavy gauge steel chassis. The s.f. and i.f.1 unit has a diecast aluminium chassis to ensure extreme rigidity, and this provides mounting points for two sub-chassis. These four units are fitted with standard 19 in. steel front panels, steel or aluminium side panels and top and bottom covers. (Power supply unit has top cover only).

11. To gain access to any chassis it is only necessary to release the four captive screws located in the corners of the front panel. The unit can then be withdrawn on extension runners to the limit of the automatic stops. From this position any chassis, with the exception of the power supply unit, can be tipped up and locked at right angles to its normal position giving easy access to the majority of the components and wiring on the underside.

12. The distribution unit components are mounted on the steel front panel or the backplate which is secured to the panel by metal pillars. The unit is not on runners and is bolted directly to the cabinet.

13. The cabinet is permanently mounted on a trolley. Four vertically mounted handles are provided, one on each side, front and rear of the cabinet. The lower part of each handle is pivoted so that it can be raised to the horizontal to form a porter bar.

Connections

Internal

14. Connections between units are made by two cableforms which are of sufficient length to permit withdrawal of units on their runners without interrupting the operation of the receiver. The cableforms are fitted with retaining clamps which anchor them securely to tie-bars on each chassis, thus preventing any strain being placed on the cable terminations.

15. Plugs and sockets on each chassis are identified by letters, and their associated cable terminations are lettered to correspond. Similar multi-pole terminations are differently orientated to prevent mis-mating.

External

16. All external connections are made to the distribution unit located at the bottom front of the receiver. A steel footguard is normally bolted to the cabinet to provide protection for the unit and connectors.

Principles of operation

S.F. and i.f.1 unit

17. Fig 3 is a simplified block diagram of the receiver.

18. The s.f. and i.f.1 unit accommodates all the circuits necessary for selection of any required frequency within the band of 2.1-27Mc/s. A calibrator, incorporating a crystal in a thermostatically controlled oven, is included.

Double frequency conversion is used to obtain a 2nd i.f. of 100kc/s.

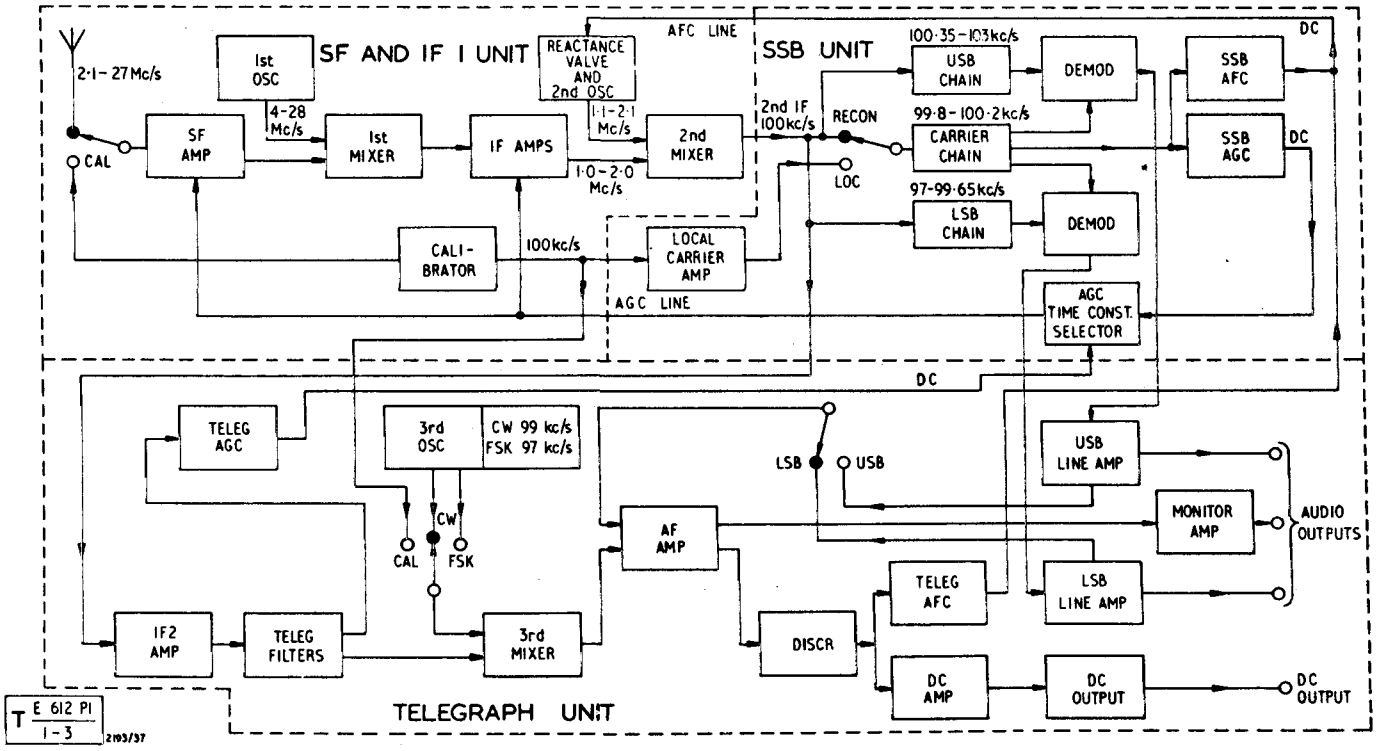

Fig 3 - Receiver, Radio, R234, simplified block diagram

19. The first oscillator is crystal controlled with an output at any selected megacycle point between 4 and 28Mc/s. The operating crystal is selected by means of a decade switching system, and it is arranged that the output frequency of the oscillator circuit is always between 1 and 2Mc/s higher than the frequency of the received signal.

20. The first mixer output frequency may lie anywhere between 1 and 2Mc/s, depending upon first oscillator and signal frequencies, and the first i.f. stages are tunable over this range.

21. The second oscillator frequency is variable over the range 1·1-2·1Mc/s. It is tuned by one section of the 4 gang variable capacitor used to tune the first i.f. amplifier stages. This arrangement results in a constant second i.f. signal centred on 100kc/s which is fed to the s.s.b. and telegraph units.

22. Automatic control of the second oscillator frequency by reactance valve is possible on telephony and f.s.k. reception.

23. Automatic gain control is applied to the s.f. and i.f.1 stages.

24. The calibrator feeds a spectrum of harmonics into the receiver antenna circuit. Marker pips appear every 100kc/s or every 10kc/s as required, throughout the s.f. range of the set.

25. The calibrator also supplies a 100kc/s signal which is used as a local carrier for demodulation purposes when propogation conditions are such that the pilot carrier cannot be reconditioned satisfactorily. This signal is also used to produce the tuning signal when calibrating.

26. For diversity reception, when two similar receivers are used, the three oscillators in the s.f. and i.f.1 unit of the slave receiver are rendered inoperative. Oscillator voltages at correct levels are supplied by the master receiver.

S.S.B. unit

27. The s.s.b. unit contains the special circuits necessary for reception of s.s.b. and i.s.b. signals. These circuits are also used when receiving d.s.b. signals.

28. The composite 2nd i.f. signal is fed to the three main sections of the unit; the carrier chain, the u.s.b. chain and the l.s.b. chain.

29. In the carrier chain the signal is amplified and fed to a crystal filter, the passband of which is 400c/s centred on 100kc/s. The output from the filter is amplified and injected into the u.s.b. and l.s.b. demodulators as a reconditioned carrier at a level determined by the system of reception in use. If necessary, this reconditioned carrier can be replaced by the local carrier produced in the calibrator.

30. In the u.s.b. chain, the i.f. signal is amplified and fed to a crystal filter, the passband of which is 100.35-103kc/s. The output from the filter is amplified and then fed to the u.s.b. demodulator together with the carrier signal. The resultant a.f. output is passed, via a cathode follower, to the u.s.b. line amplifier which is located in the telegraph unit.

31. The circuits of the l.s.b. and u.s.b. chains are identical. The passband of the l.s.b. filter is 97-99.65kc/s.

32. Also included in the s.s.b. unit are the circuits for a.g.c. time constant selection, s.s.b. a.g.c., s.s.b. a.f.c., and tuning indication.

Telegraph unit

33. The telegraph unit contains the special circuits required for c.w. and f.s.k. reception.

34. The composite second i.f. signal is amplified and then fed to a filter with a nominal bandwidth of 1kc/s centred on 100kc/s. The signal is then further amplified and applied to either a 400c/s passband filter or to an attenuator network which has the same insertion loss as the filter. After further amplification the signal is fed into the third mixer.

35. The third oscillator, which is crystal controlled, runs at 99kc/s for c.w. reception or 97kc/s for f.s.k. reception. The output from this stage is injected into the third mixer, together with the filtered second i.f. signal.

36. When receiving c.w. the mixer output at the difference frequency of 1kc/s is fed to the a.f. amplifier and thence to the monitor amplifier which drives a loudspeaker or headset.

37. For f.s.k. reception, the 100kc/s second i.f. signal and the 97kc/s third oscillator signal produce a mixer output centred on 3kc/s, which is fed to the a.f. amplifier. After amplification, the 3kc/s signal (third i.f.) is fed to the signal level indicating circuit and to the discriminator via a driver stage.

38. The discriminator is tuned for a cross-over frequency of 3kc/s. The output from this stage, which consists of mark and space potentials equally displaced about earth, is used for signal and a.f.c. purposes.

39. Following the signal path, the discriminator output is coupled to a d.c. amplifier and thence, after filtering and limiting, to a d.c. output stage. The f.s.k. output from this stage activates a polarized relay external to the receiver.

40. A.F.C. voltage for feeding back to the reactance valve controlling the second oscillator frequency is derived from the discriminator output, the magnitude of the control voltage being proportional to the amount off tune, and the polarity being determined by the direction off tune. An f.s.k. tuning indicator circuit with a centre zero front panel mounted meter indicates the sense and extent of the correcting voltage being applied to the reactance valve.

41. When checking calibration, a signal from the 100kc/s calibrator oscillator, together with the 100kc/s second i.f. signal are injected into the third mixer, If the receiver is correctly tuned to a calibration signal fed into the antenna circuit, the second i.f. is exactly 100kc/s and there is therefore no output from the mixer. If the receiver is slightly mistuned, the i.f. will differ from its nominal 100kc/s resulting in a mixer output at audio frequency which is fed to the speaker or headset via the a.f. and monitor amplifiers.

42. The telegraph unit also accommodates the circuits for manual h.f. and audio gain controls, system switching, telegraph a.g.c. sideband line amplifiers and a.f.c. and signal combining. The combining circuits are fully utilized only when the receiver is working in dual diversity.

Power supplies

43. The power supply unit provides all the a.c. and d.c. supplies needed by the receiver.

44. A single phase input of voltage 100-130V or 200-250V, 45-65c/s is required. Power consumption is approximately 400VA.

45. An additional supply unit, mounted on the main supply unit chassis, provides a stabilized d.c. heater voltage for selected valves in the s.f. and i.f.1 units.

46. H.T. supply monitoring facilities are provided by a selector circuit and a front panel meter.

Controls and Indicators

47. The controls and indicators of the various units are listed and briefly

described in Tables 1, 2, 3, 4 and 5. Each unit has a code letter which prefixes the individual item reference in the tables. The coding is as follows:

A S.F. and i.f.1 unit

B S.S.B. unit

C Telegraph unit

D Power supply unit

E Distribution unit

48. Controls are colour coded in the following manner, and the coding is included in columns 1 of the tables:

Black: Tuning and frequency setting controls

Red: Service and power switching

Yellow: Metering and monitoring controls.

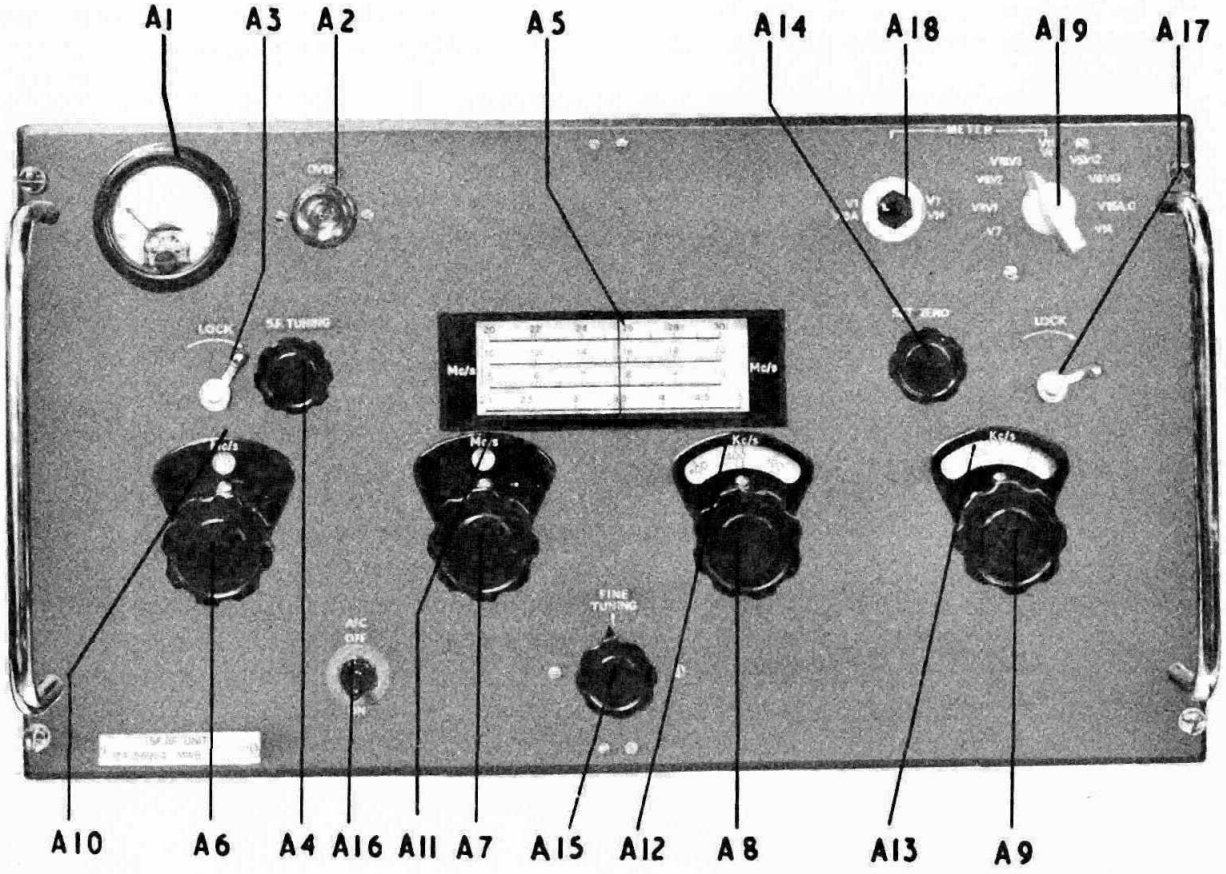

Fig 4 - Controls and indicators, s.f. and i.f.1 unit

Table 1 - Controls and indicators - s.f. and i.f.1 unit (A)

Ref	Title	Function
	External	
A1	Meter (M1)	Indicates valve current as selected by SE (A 18) and SD (A 19)
A2	OVEN lamp (ILP1)	On when oven is heating
A3	LOCK	Mechanically locks the s.f. tuning control
A4 (Black)	S.F. TUNING	Adjusts ganged capacitors C1, C2 and C3 to tune s.f. stages. Also operates the s.f. dial pointer (A5) and SC
A5	S.F. tuning dial and pointer	Indicate the frequency to which the s.f. circuits are tuned

Table 1 - (cont)

Ref	Title	Function
	External	
A6 (Black)	Mc/s coarse control (SA)	Select s.f. inductances, 1st oscillator anode circuit capacitors, buffer/multiplier anode circuit inductances and capacitors, and lamps for s.f. tuning dial illumination
A7 (Black)	Mc/s fine control (SB)	
A8 (Black)	Kc/s coarse control	Adjust gang capacitors C45, C46, C47 and C48 to tune i.f.1 amplifier and 2nd oscillator
A9 (Black)	Kc/s fine control	
A10	Mc/s coarse scale	Indicate frequency to which the receiver is tuned. The calibrations of the four scales are additive
A11	Mc/s fine scale	
A12	Kc/s coarse scale	
A13	Kc/s fine scale	
A14 (Black)	SET ZERO	Adjusts cursor of kc/s fine scale. For use when utilizing in-built calibrator
A15 (Black)	FINE TUNING (RV1)	Adjusts bias conditions of reactance valve to fine tune the 2nd oscillator
A16 (Red)	A.F.C. switch (SF)	Switches reactance valve control grid to a.f.c. voltage or to earth
A17	LOCK	Mechanically locks the kc/s controls
A18 (Yellow)	METER valve bank selector (SE)	Select valve current to be monitored by front panel meter (A1)
A19 (Yellow)	METER valve selector (SD)	
	Internal, pre-set	
RV2	Multivibrator control	Varies time constant of 10kc/s multivibrator frequency determining circuit to adjust repetition frequency

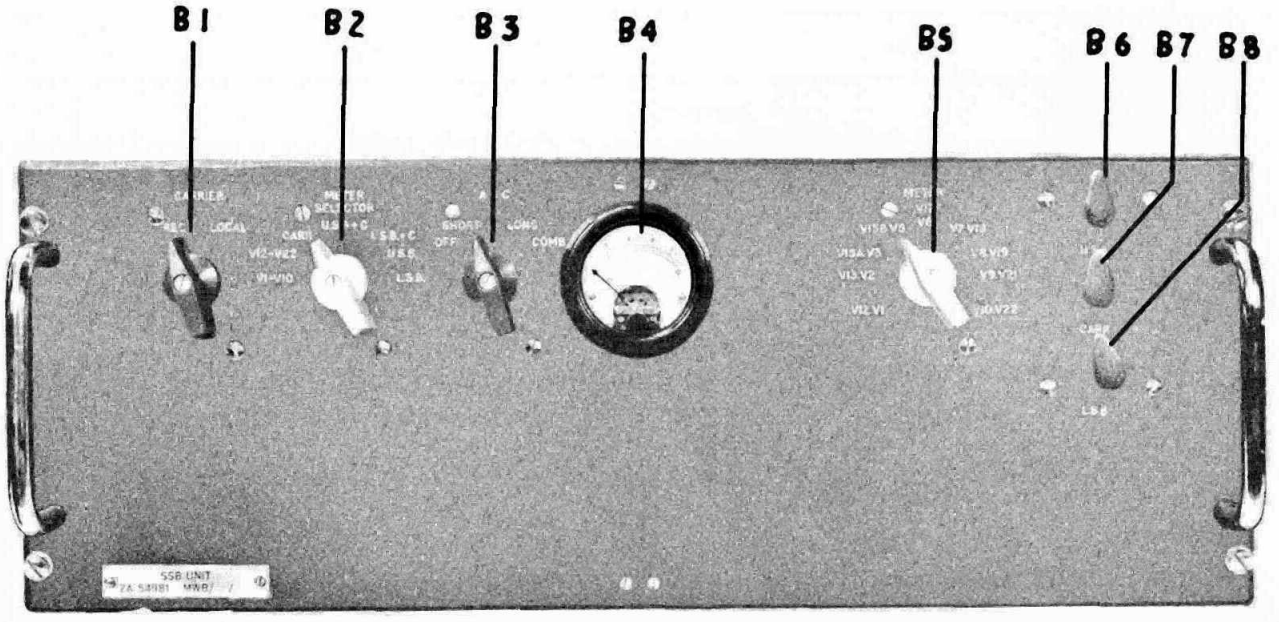

Fig 5 - Controls and indicators, s.s.b. unit

Table 2 - Controls and indicators - s.s.b. unit (B)

Ref	Title	Function
	External	
B1 (Red)	CARRIER switch (SB)	Selects carrier system to be used (Reconditioned or local)
B2 (Yellow)	METER SELECTOR (SC)	Selects valve groups, or carrier + sideband or sideband levels to be indicated on front panel meter. Interconnected with METER switch SA (B5)
B3 (Red)	A.G.C. SELECTOR (SE)	Switches a.g.c. to earth or alters a.g.c. circuit time constant. COMB position used only when receiver is working in diversity
B4	METER (M1)	Indicates valve currents, carrier or sideband levels as selected by meter switches SC (B2) and SA (B5)
B5 (Yellow)	METER switch (SA)	Selects valve feed currents, as marked on front panel, to indicate on Meter M1 (B4). Interconnected with SC (B2)

Table 2 - (cont)

Ref	Title	Function
	External	
B6	U.S.B. control (RV1 pre-set)	Adjusts gain of u.s.b. amp. V2
B7	CARR control (RV3 pre-set)	Adjusts gain of carrier amp. V7
B8	L.S.B. control (RV6 pre-set)	Adjusts gain of l.s.b. amp. V18
	Internal, pre-set	
	U.S.B. carrier gain control (RV2)	Adjusts gain of u.s.b. reconditioned/local carrier amp. V6
	Local carrier gain control (RV4)	Adjusts gain of local carrier amp. V12
	Set zero control (RV5)	Adjusts cathode bias of tuning indicator V15 so that under no signal conditions output to meter M2 (C3) is zero
	L.S.B. carrier gain control (RV7)	Adjusts gain of l.s.b. reconditioned/local carrier amp.V22
	S.S.B. and d.s.b. carrier level controls (RV8 and RV9)	Adjust carrier amp. gain for s.s.b. and d.s.b. operation when switched by system switch (C9)

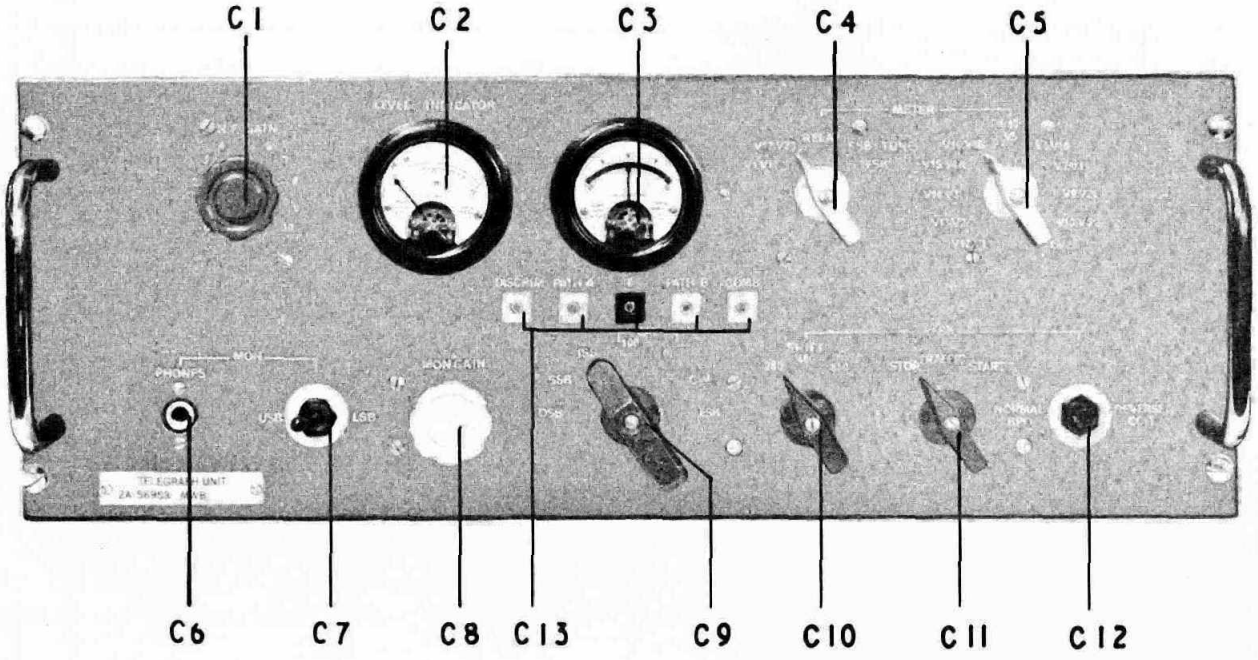

Fig 6 - Controls and indicators, telegraph unit

Table 3 - Controls, indicators and sockets - telegraph unit (C)

Ref	Title	Function
C1 (Red)	H.F. GAIN (RV4)	Varies the negative bias which is applied to the a.g.c. line in addition to the a.g.c. voltage
C2	LEVEL INDICATOR (M1)	Indicates strength of received f.s.k. signal
C3	Centre-zero meter (M2)	Monitors valve feed and telegraph relay current as selected by SC (C4) and SE (C5). Also acts as f.s.k. and s.s.b. tuning indicator
C4 (Yellow)	METER switch (SC)	Selects valve current to be monitored by M2 (C3) in co-ordination with SB (C5), or switches meter to measure telegraph relay current or to act as tuning indicator

Table 3 - (cont)

Ref	Title	Function
	External	
C5 (Yellow)	METER, selector switch (SB)	Selects with SC (C4) the valve feed current to be monitored
C6	MON PHONES (JKA)	For connection of high impedance headset to the monitor amplifier output
C7 (Yellow)	MON switch (SD)	Connects either the u.s.b. or l.s.b. audio signal to the monitor amplifier
C8 (Yellow)	MON GAIN (RV3)	Adjusts the audio output level of the monitor amplifier
C9 (Red)	System switch (SA)	Selects the circuits appropriate to the system of transmission in use
C10 (Red)	F.S.K. SHIFT switch (SF)	Selects the clamp circuit (RV7-12) for correct working at the operational shift frequency
C11 (Red)	F.S.K. test switch (SG)	Connects the signal or a steady STOP or START (mark or space) test potential to the signal combiner stage
C12 (Red)	F.S.K. polarity switch (SE)	Changes the polarity of the f.s.k. signal to conform with BPO or CCIT standards when SG (C11) is at TRAFFIC
C13	Sockets: DISCRIM PATH A PATH B COMB E	Monitoring points for telegraph waveforms
	Internal, pre-set	
	U.S.B. gain control (RV1)	Adjusts u.s.b. audio output level
	L.S.B. gain control (RV2)	Adjusts l.s.b. audio output level
	Set zero, tuning indicator (RV5)	Balances f.s.k. tuning indicator stage under no signal conditions
	Set zero, comparator (RV6)	Balances comparator stage

Table 3 - (cont)

Ref	Title	Function
	Clamp control, 850c/s shift (RV7) Clamp control, 400c/s shift (RV8) Clamp control, 280c/s shift (RV9) Clamp control, 850c/s shift (RV10) Clamp control, 400c/s shift (RV11) Clamp control, 280c/s shift (RV12)	Adjust the a.f.c. comparator reference voltages
	Set zero, a.f.c. comparator (RV13)	Balances the a.f.c. comparator stage under no signal conditions
	Signal bias control (RV14)	Adjusts slicing level of the limiter preceding the d.c. output stage
	I.F. gain control (RV15)	Adjusts gain of i.f. strip by variation of bias of the first i.f.2. amplifier
	Filter switches (SH and SJ)	Separate double pole change-over switches to be operated simultaneously. To be set to 400c/s position when operating f.s.k. with 280c/s shift. FIL 2 then in circuit. For all other operating conditions, switch to 1000c/s

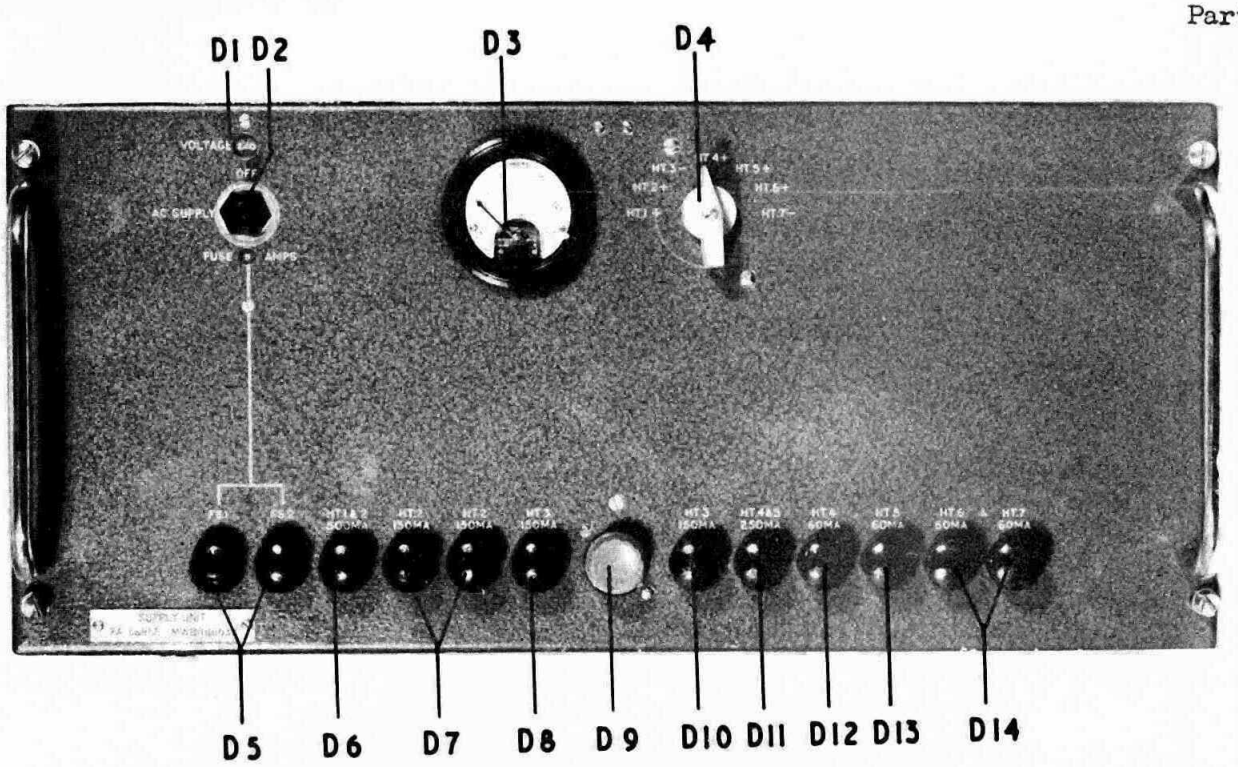

Fig 7 - Controls, indicators and fuses, power supply unit

Table 4 - Controls - indicators and fuses - power supply unit (D)

Ref	Title	Function
	External	
D1	Voltage indicating disc	Indicates input voltage for which mains transformer primary windings are connected. Also indicates correct rating for FS1 and FS2 (D5)
D2	AC SUPPLY switch (SA)	Switches a.c. input from FS1 and FS2 to mains transformer primaries
D3	Meter M1	Indicates the voltage of the h.t. supply to which it is connected by SB (D4)
D4	SB	Selects h.t. supply to be monitored by M1 (D3)
D5	FS1 and FS2	Mains input fuses. Correct rating indicated by voltage indicating disc (D1) Ratings: For 100-130V a.c. operation: 10A For 200-250V a.c. operation: 5A
D6	FS3	Fuse in common a.c. input circuit for HT1 and HT2 supplies. Rating: 500mA anti-surge

Table 4 - (cont)

Ref	Title	Function
	External	
D7	FS4 and FS5	Fuses in HT 2 supply Ratings: FS4: 150mA anti-surge FS5: 150mA
D8	FS6	Fuse in a.c. input circuit for HT3 supply Rating: 150mA anti-surge
D9	ILP1	Indicates that AC SUPPLY switch is on and that T1 heater transformer is energized
D10	FS7	Fuse in HT3 supply Rating: 150mA
D11	FS8	Fuse in common a.c. input circuit for HT4 and HT5 supplies Rating: 250mA, anti-surge
D12	FS9	Fuse in HT4 supply Rating: 60mA
D13	FS10	Fuse in HT5 supply Rating: 60mA
D14	FS11 and FS12	Fuses in common a.c. input circuit for HT6 and HT7 supplies Rating: 60mA anti-surge
	Internal, pre-set	
	Output control (RV1)	Adjusts the output level of the 12.6V d.c. stabilized l.t. supply

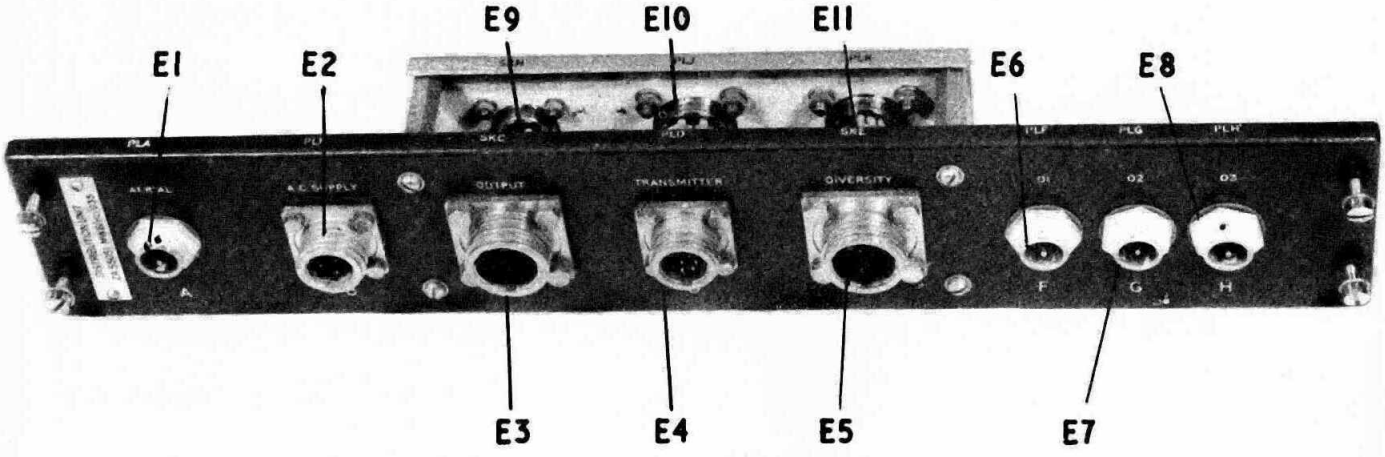

Fig 8 - Terminations, distribution unit

Table 5 - Plugs and sockets - distribution unit (E)

Ref	Title		Function
	External		
E1	AERIAL (PLA)	A	Antenna input plug
E2	AC SUPPLY (PLB)	B	AC mains input plug
E3	OUTPUT (SKTC)	C	Connects audio and telegraph outputs to control indicator and desensitizing voltage from control indicator to receiver
E4	TRANSMITTER (PLD)	D	Connects sidetone from transmitter to receiver audio circuits
E5	DIVERSITY (SKTE)	E	Connects a.f.c., a.g.c. and signal circuits to control indicator for commoning when two receivers are acting in dual diversity
E6	01 (PLF)	F	Connects 1st oscillator circuits of two receivers acting in dual diversity. This outlet must be terminated by a 75Ω dummy load when the R234 is working independently
E7	02 (PLG)	G	Connects 2nd oscillator circuits of two receivers acting in dual diversity. This outlet must be terminated by a 75Ω dummy load when the R234 is working independently
E8	03 (PLH)	H	Connects 100kc/s crystal oscillator circuits of two receivers acting in dual diversity, This outlet must be terminated by a 75Ω dummy load when the R234 is acting independently
	Rear		
E9	SKTH		Interconnecting socket between PLB (E2) and power supply unit
E10	PLJ		Interconnecting plug between SKTC (E3) and the telegraph unit
E11	PLK		Interconnecting plug between PLD (E4) and SKTE (E5) and the telegraph unit

DETAILED TECHNICAL DESCRIPTION

General

49. The receiver R234 comprises the following units:-

A	SF and i.f.1 unit	Type 5414B
B	S.S.B. unit	Type 5415A
C	Telegraph unit	Type 6637A
D	Power supply unit incorporating Power supply unit	Type 7554A Type 5441A
E	Distribution unit	Type 5417A

50. The R234 can function independently or it can be used as a master or slave receiver in a dual diversity receiving system using two identical sets. Diversity operation necessitates circuit changes in the s.f. and i.f.1 unit of the slave.

S.F. and I.F.1 UNIT, TYPE 5414B
(Fig 2503-2507)

General

51. The s.f. and i.f.1 unit consists basically of a double superheterodyne receiver and a crystal calibrator which carry out the following functions:-

(a) Signal frequency selection.

(b) Conversion of the selected signal frequency to an intermediate frequency of 100kc/s

(c) Generation of calibration signals throughout the tuning range of the receiver

(d) Generation of a local carrier to replace the reconditioned pilot carrier when required.

52. The main physical features of the unit are shown in Fig 9. The sub-chassis on the left accommodates the signal frequency and first oscillator circuits, whilst the first i.f. amplifier and second oscillator components are mounted in the centre. The large cylindrical screening can located immediately behind the front panel houses the tuning inductance of the second oscillator, to the left of which can be seen the 4 gang variable capacitor which tunes the first i.f. amplifiers and second oscillator. Reactance valve V7 and second oscillator buffer amplifier V14 are mounted on the underside of the chassis, together with the majority of smaller components. Calibrator components are mounted on the sub-chassis adjacent to the right wall of the unit, the plug-in crystal oven being clearly visible at the rear.

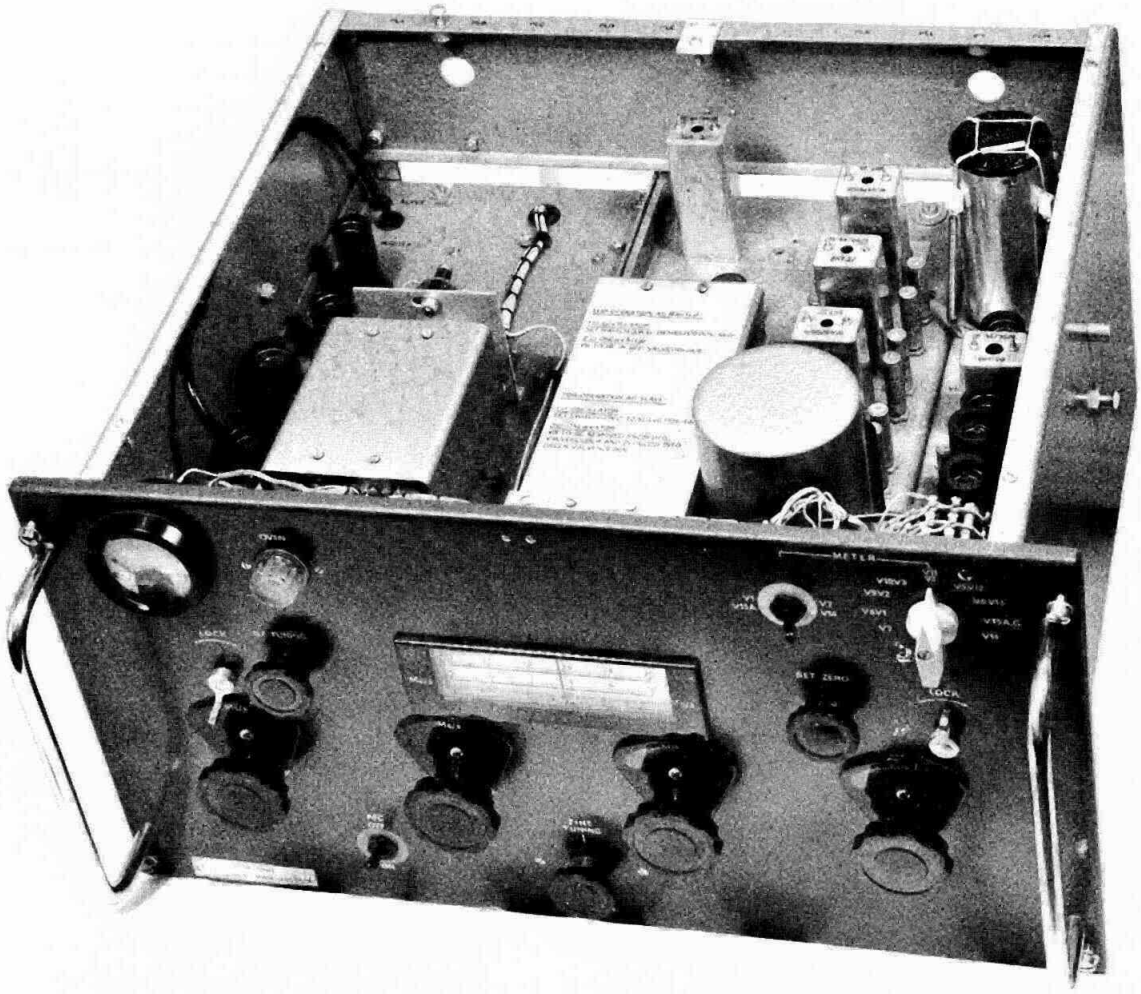

Fig 9 - S.F. and i.f.1 unit, general view

RV2, 10kc/s multivibrator frequency control, is not visible. It is located at the front panel end of the sub-chassis and is accessible from the top.

53. Cast aluminium boxes are used for screening the underside of the calibrator sub-chassis and the signal frequency and first oscillator circuits.

54. Connections to the unit are made by Mk 4B plugs and Burndept co-axial plugs mounted on the rear of the chassis.

55. Fig 10 is a block diagram of the unit.

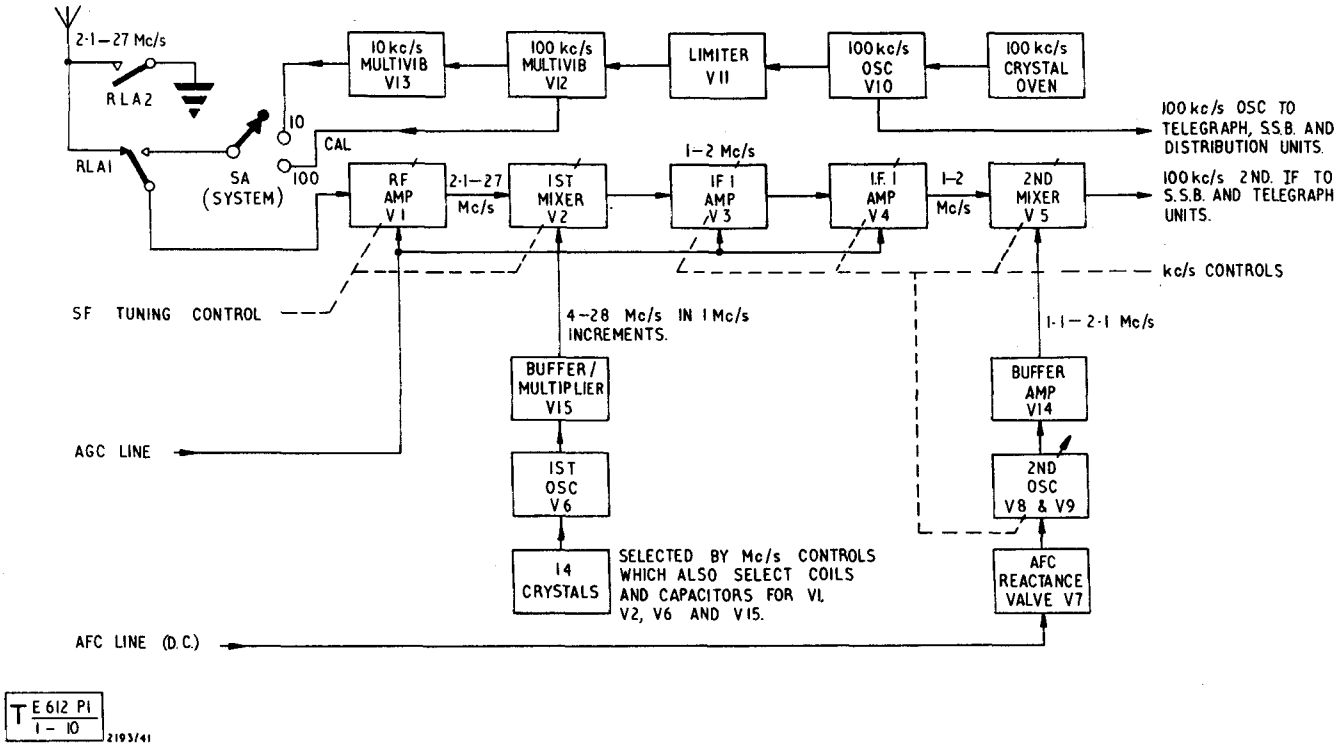

Fig 10 - S.F. and i.f.1 unit, block diagram

Frequency selection

56. Fig 11 shows the relationship between the front panel controls and the frequency selecting circuits.

Mc/s controls

57. Multi-bank rotary switches SA and SB, together with their associated dials, are operated by the two controls marked Mc/s.

Frequency band switching is effected by SA and SB which select:

(a) First oscillator crystals and anode tuned circuits

(b) Buffer/multiplier anode tuned circuits

(c) Signal frequency inductances

(d) Signal frequency dial illuminating lamps.

SA is a 3 position switch with scale calibrations of 0, 10 and 20. SB has 10

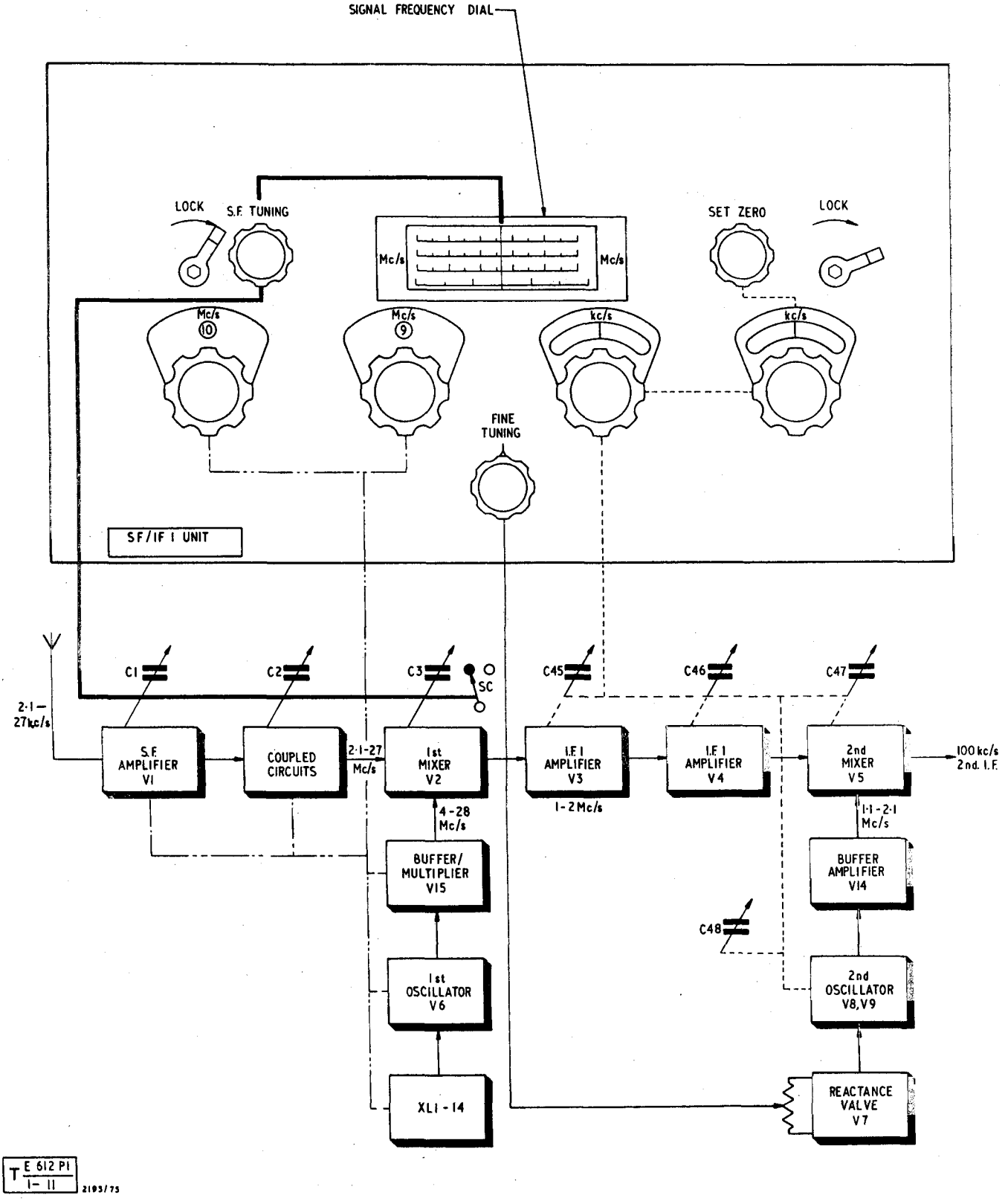

Fig 11 – Frequency selection, control functions, block diagram

positions with scale calibration 0-9 inclusive. The calibrations of the two scales are additive.

Kc/s controls

58. The fine and coarse kc/s controls drive ganged capacitors C45, C46 C47 and C48 through a train of anti-backlash gears. The two controls are coupled by a 10:1 reduction drive. The peripheral scale of the coarse control is calibrated 0-1000 in steps of 100, whilst the fine scale is calibrated 0-100 in steps of 10 with nine sub-divisions between each step. The fine scale viewing window is fitted with a movable cursor which is adjusted by the SET ZERO control.

59. The first mixer (V2) output frequency lies between 1 and 2Mc/s depending upon the output frequency of V15 and the incoming signal frequency. C45, C46 and C47 tune the i.f.1 amplifiers over the range 1-2Mc/s. C48 tunes the second oscillator between 1.1-2.1Mc/s. The outputs from the i.f.1 amplifier and second oscillator buffer amplifier (V14) are injected into the second mixer (V5), and the resultant difference frequency of 100kc/s is developed across V5 anode load and is the second i.f.

60. A locking device is provided for the kc/s drive mechanism.

S.F. TUNING control

61. The S.F. TUNING control drives ganged capacitors C1, C2, C3, the s.f. dial pointer and SC, which is ganged to the capacitors. The s.f. inductances, which are selected by SA and SB, are tuned by C1, C2 and C3.

62. Should the s.f. circuits be inadvertently tuned towards an image signal, the h.t. supply to the screens of the i.f. amplifiers is removed by SC, thus muting the receiver.

63. There are four frequency range scales on the s.f. dial. These are calibrated as follows:-

2.1-5Mc/s
5-10Mc/s
10-20Mc/s
20-30Mc/s

64. Eight midget single pole lamps, contained in two lampholders provide side illumination for the scales. The lamps are switched on in pairs by SA and SB.

65. A locking device is provided for the tuning mechanism.

FINE TUNING control

66. The FINE TUNING control allows precise adjustment of second oscillator frequency by slight variation of the bias conditions of the reactance valve.

67. Table 6 gives examples of frequency relationships within the s.f. and i.f.1 unit for a number of different signal frequencies.

Table 6 - Frequency selection - example frequencies

Signal frequency Mc/s	Mc/s dials Mc/s		Kc/s dials kc/s		1st Osc crystal frequency Mc/s	Buffer/ multiplier output frequency Mc/s	1st i.f. Mc/s	2nd Osc frequency Mc/s	2nd i.f. kc/s
	SA	SB							
2.1	0	2	100	0	4	4	1.9	2.0	100
5.678	0	5	>600	78	7	7	1.322	1.422	100
13.285	10	3	>200	85	5	15	1.715	1.815	100
26.0	20	6	0	0	14	28	2.0	2.1	100
27	20	6	1000	0	14	28	1.0	1.1	100

S.F. amplifier V1

68. Fig 12 is a simplified diagram of the s.f. amplifier.

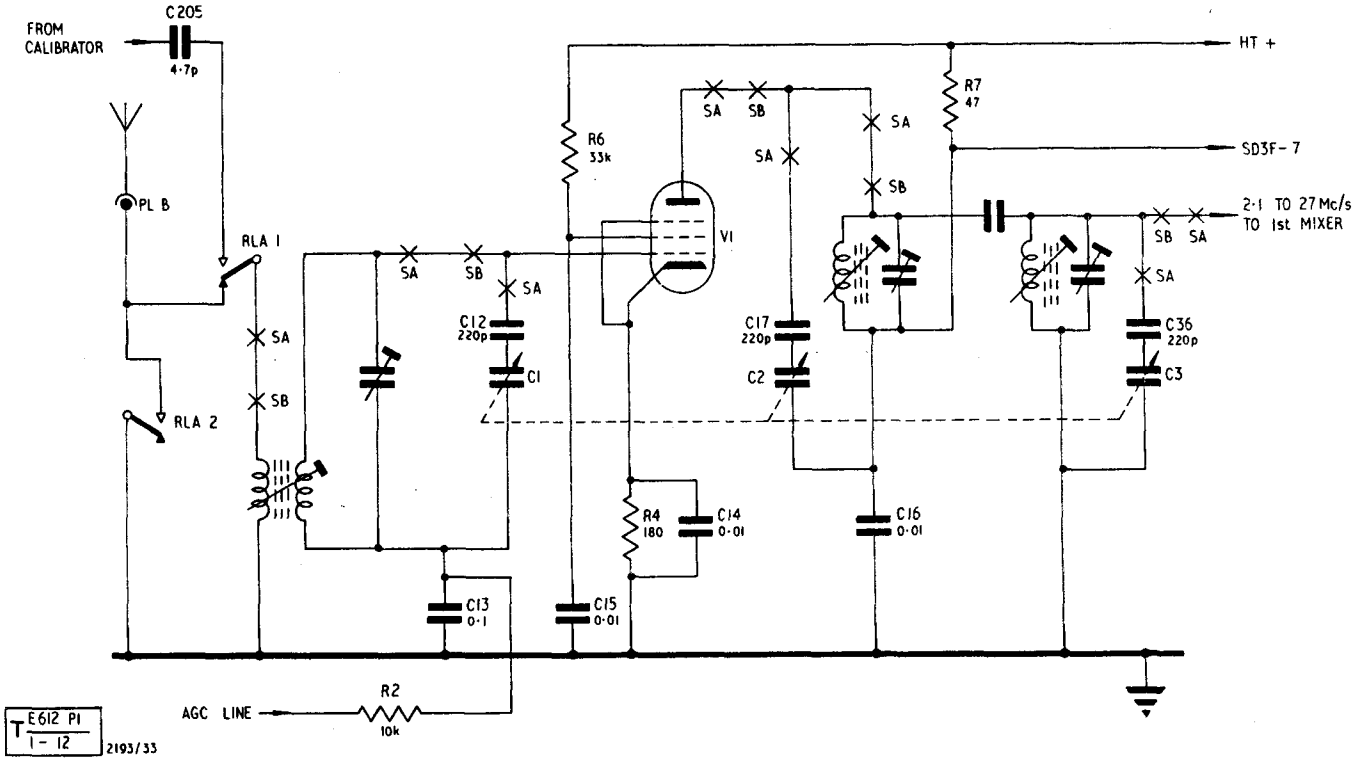

Fig 12 - S.F. amplifier, simplified circuit diagram

69. The input to the amplifier, which may be from the antenna via PLB or from the crystal calibrator via C205, is transformer coupled to V1 control grid. The input is selected by RLA which, when energized, connects the calibrator input to the input transformer primary in place of the antenna input which is then earthed. The relay is energized when the set is switched to CAL or when the desensitizing circuit (telegraph unit, para 304) is operated.

70. In addition to normal a.g.c. the variable manual gain control bias (HF GAIN, telegraph unit, para 295) is applied to the a.g.c. line. When the desensitizing circuit is operated, a fixed bias of approximately -4CV replaces the manual gain control voltage.

71. On frequency bands 20-27Mc/s, SA in position 3, the swing of C1, C2 and C3 (284pF max) is reduced by series capacitors C12, C17 and C36.

72. All s.f. circuit switching is carried out by SA and SB operated by the Mc/s controls. The relationship between the switch positions and the Mc/s scales is shown in Tables 7 and 8.

Table 7 - SA position with respect to scale reading

SWITCH POSITION	1	2	3
COARSE MC/S SCALE READING	0	10	20

Table 8 - SB position with respect to scale reading

SWITCH POSITION	1	2	3	4	5	6	7	8	9	10
FINE MC/S SCALE READING	0	1	2	3	4	5	6	7	8	9

73. Full functional details of the s.f. switching wafers of SA and SB are contained in Tables 9 and 10.

Table 9 - S.F. switching details - SA

WAFER	SWITCHING	POSITION	CONNECTIONS MADE
1F	S.F. input from RLA1	1	To L7 or L5 via SB2F
		2	To L3
	and	3	To L1
	V1 control grid	1	To L6 or L8 via SB1F
		2	To L4
		3	To L2
1B	Windings not selected by SA1F	ALL	To earth
2F	C12	1	short circuit across C12
		2	
		3	Not effective. C12 in series with C1
3F	V1 anode	1	To L11 or L12 via SB3B and SB3F
		2	not effective
		3	
		1	not effective
		2	
		3	Short circuit L10 or L11 or L12 via SA3B and SB4B
3B	C2	1	To L12 or L11 via SB4F
		2	To L10
		3	To L9 with C17 in series
4F	C36	1	short circuit across C36
		2	
		3	Not effective, C36 in series with C3
5F	V2A control grid	1	To L16 or L15 via SB5F
		2	To L14
		3	To L13
5B	The windings not selected by SA5F	ALL	Short circuit to earth
9F	6.3V from PLA-G) PLA-H)	1	To ILP2 and ILP3 or ILP4 and ILP5 via SB11F
		2	To ILP8 and ILP9
	and	3	To ILP6 and ILP7
	HT1 (+200V)	ALL	To V3 and V4 screens via SB12F or SB12R and SC

Table 10 - S.F. switching details - SB

WAFER	SWITCHING	POSITION	CONNECTIONS MADE
1F	Antennatransformer secondary windings	1-2 3-5 6-10	Not effective L8 to SA1F L6 to SA1F
1B	The windings not selected by SB1F	ALL	To earth
2F	Antennatransformer primary SB2F	1-2 3-5 6-10	Not effective L7 to SA1F L5 to SA1F
2R	The windings not selected by SB2F	ALL	To earth
3F	V1 anode tuned circuit	1-2 3-5 6-10	Not effective L12 to SA3F L11 to SA3F
3B			
4F	V1 anode tuned circuit	1-2 3-5 6-10	Not effective L12 to SA3B L11 to SA3B
4B	The winding not selected by SA4B	ALL	Short circuit
5F	V2A control grid	1-2 3-5 6-10	To earth L16 to SA5F L15 to SA5F
5B	The winding not selected by SB5F	ALL	To earth
11F	Dial lamps	1-2 3-5 6-10	Not effective ILP4 and ILP5 to SA9F ILP2 and ILP3 to SA9F
12F)) 12B)	HT1 (+200V) from SA9F		To V3 and V4 screens via SC

First oscillator V6 and buffer/multiplier V15

74. V6 is a pentode connected as an electron coupled crystal oscillator of the Pierce type with the crystal connected between the screen and control grids (Fig 13 and 2504b).

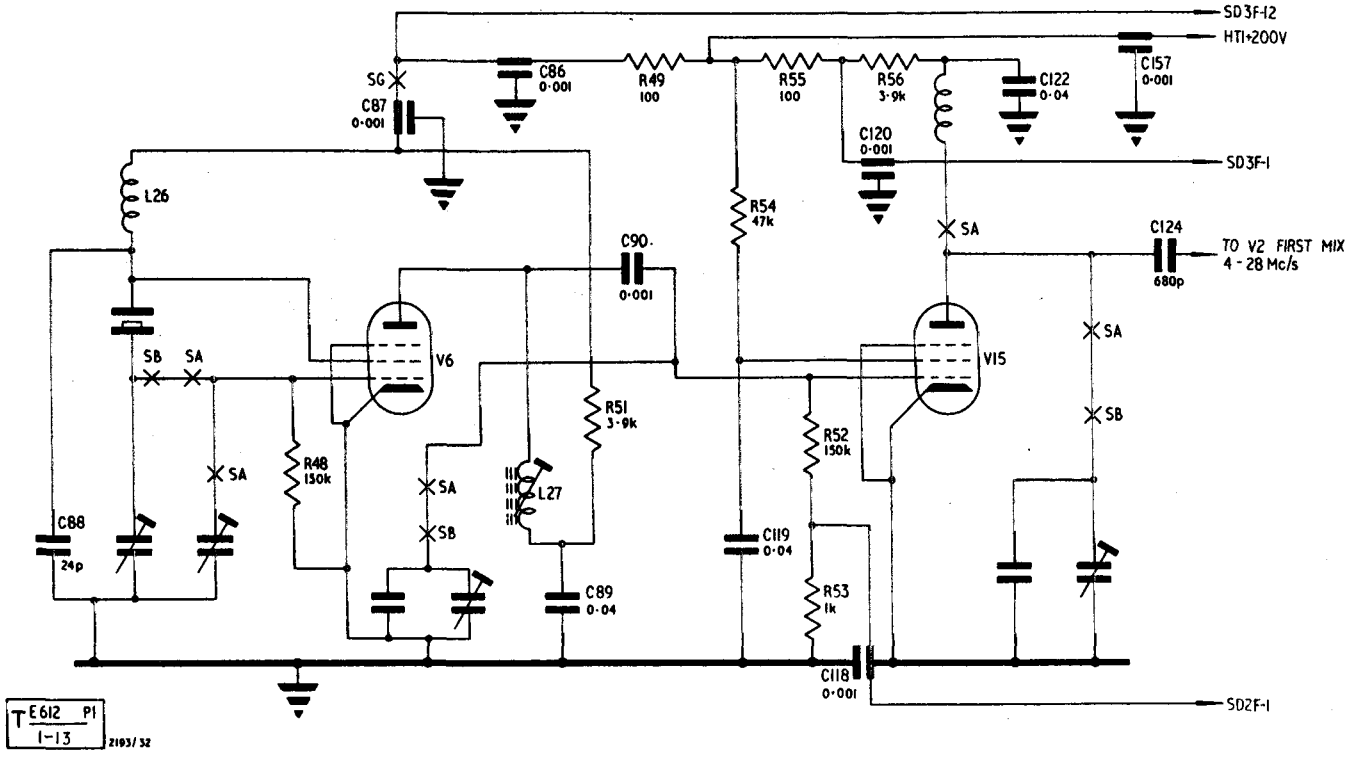

Fig 13 - First oscillator and buffer amplifier, simplified circuit diagram

75. Fourteen crystals and associated trimming capacitors, selected by SA and SB, enable the combination of oscillator and buffer/multiplier to cover the required frequency range of 4 to 28Mc/s in 25 ranges each separated by 1Mc/s. Nine of the crystals are selected for use on more than one range. For example, XL11 is switched into circuit when the Mc/s dials are set to 0, 5 or to 10, 9. (See Table 11). To compensate for the change in stray capacitance which occurs in V6 grid circuit when the position of SA is changed, trimming capacitors C83, C84 and C85 are selected and connected between V6 grid and earth by SA.

76. The oscillator anode circuit, consisting of L27 and capacitors selected by SA and SB, is tuned to crystal frequency on each range.

77. The bases of V6 and V15 are in screened compartments and all supply voltages for both valves are via ceramic feed-through capacitors. HT for the oscillator is controlled by the MASTER/SLAVE switch SG which must be at MASTER when the receiver is working independently or as a master equipment in a dual diversity station.

78. On the eight lowest frequency ranges, V15 anode load is r.f. choke L28, and the output at crystal frequency is coupled to the mixer by C124. On the remaining ranges the anode circuit, selected by SA and SB, is tuned to crystal frequency or its second or third harmonic. On all ranges V15 output frequency is higher than that of the incoming signal.

79. Table 11 details crystal selection and shows the relationship between crystal and multiplier output frequencies.

Table 11 - Crystal selection and oscillator and buffer/multiplier output frequencies

Mc/s Dials		Crystal		Multiplier output frequency Mc/s	Mc/s Dials		Crystal		Multiplier output frequency Mc/s
SA	SB	Circuit ref, XL	Frequency Mc/s		SA	SB	Circuit ref, XL	Frequency Mc/s	
0	2	14	4	4	10	4	10	8	16
0	3	13	5	5	10	5	9	8.5	17
0	4	12	6	6	10	6	8	9	18
0	5	11	7	7	10	7	7	9.5	19
0	6	10	8	8	10	8	6	10	20
0	7	8	9	9	10	9	11	7	21
0	8	6	10	10	20	0	5	11	22
0	9	5	11	11	20	1	4	11.5	23
10	0	12	6	12	20	2	10	8	24
10	1	2	13	13	20	3	3	12.5	25
10	2	1	14	14	20	4	2	13	26
10	3	13	5	15	20	5	8	9	27
					20	6	1	14	28

80. In addition to anode current monitoring, provision is made to monitor V15 grid current as a check on the drive from V6. For this test, the front panel meter is switched across R53, C118 decoupling the feed out to SD.

81. The temperature co-efficient of the oscillator is approximately 2 parts in 10^6 per degree centigrade.

Oscillator switching

82. The functions of the oscillator and buffer/multiplier switching wafers of SA and SB are detailed in Tables 12 and 13.

WAFER	SWITCHING	POSITION	CONNECTIONS MADE TO
6F	V15 anode	1	L28
		2	L29 and SB6F
	and	3	L30 and SB6B
	C124 coupling capacitor	1	L28
		2	C121
	and	3	C123
	L28	1	Not effective
		2	Short circuit
	L28 and L29	3	Short circuit

Table 12 - Oscillator and buffer/multiplier switching - SA

Table 12 - (cont)

WAFER	SWITCHING	POSITION	CONNECTIONS MADE TO
7F	V6 anode	1	SB7F
		2	SB7R
		3	SB8F
8F	V6 control grid	1	C85 and SB9F
		2	C84 and SB9B
		3	C83 and SB10F

Table 13 - Oscillator and buffer/multiplier switching - SB

WAFER	SWITCHING	POSITION	CONNECTIONS MADE TO
6F	L29	1	C141 and C142
		2	C139 and C140
		3	C138 and C137
		4	C136 and C135
		5	C134 and C133
		6	C132 and C131
		7	C130 and C129
		8	C128 and C127
		9	C126
		10	C125
6B	L30	1	C155 and C156
		2	C153 and C154
		3	C151 and C152
		4	C149 and C150
		5	C147 and C148
		6	C145 and C146
		7	C143 and C144
		8	
		9	
		10	
7F	SA7F-1	1	C116 and C117
		2	
		3	
		4	C113, C114 and C115
		5	C111 and C112
		6	C109 and C110
		7	C107 and C108
		8	C103 and C104
		9	C99 and C100
		10	C97 and C98

Table 13 - (cont)

WAFER	SWITCHING	POSITION	CONNECTIONS MADE TO
7B	SA7F-2	1	C111 and C112
		2	C92
		3	C91
		4	C114 and C115
		5	C107 and C108
		6	C105 and C106
		7	C103 and C104
		8	C101 and C102
		9	C99 and C100
		10	C109 and C110
8F	SA7F-3	1	C97 and C98
		2	C95 and C96
		3	C107 and C108
		4	C93 and C94
		5	C92
		6	C103 and C104
		7	C91
		8	
		9	
		10	
9F	SA8F-10	1	XL 14
		2	
		3	
		4	XL13 and SB9B
		5	XL12 and SB9B
		6	XL11 and SB9B
		7	XL10, SB9B and SB10F
		8	XL8, SB9B and SB10F
		9	XL6 and SB9B
		10	XL5 and SB10F
9B	SA8F-11	1	XL12 and SB9F
		2	XL2 and SB10F
		3	XL1 and SB10F
		4	XL13 and SB9F
		5	XL10, SB9F and SB10F
		6	XL9
		7	XL8, SB9F and SB10F
		8	XL7
		9	XL6 and SB9F
		10	XL11 and SB9F
10F	SA8F-12	1	XL5 and SB9F
		2	XL4
		3	XL10, SB9B and SB9F
		4	XL3
		5	XL2 and SB9B
		6	XL8, SB9B and SB9F
		7	XL1 and SB9B
		8	
		9 and 10	

First Mixer, V2A and V2B

83. Fig 14 is a simplified circuit of the first mixer stage which uses a double triode connected in cascode across the H.T. supply.

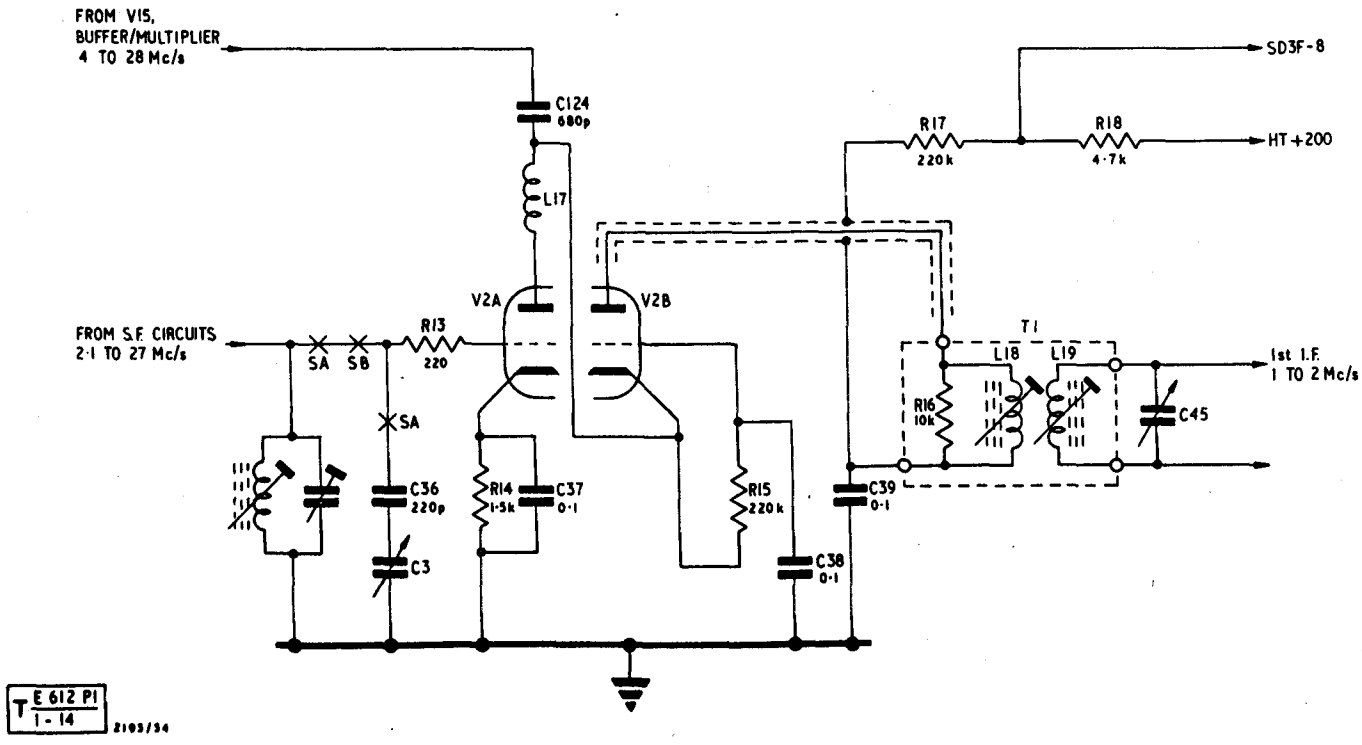

Fig 14 - First mixer, simplified circuit diagram

84. With this circuit it is possible to obtain low noise performance with overall gain approaching that of a pentode stage. In addition, satisfactory operation is achieved with a low value of oscillator injection voltage (in the region of 1V).

85. V2A is a grounded cathode triode amplifier followed by a grounded grid triode, V2B. Matching between the two sections is achieved by a network made up of L17, the anode/cathode capacitance of V2a and the cathode/grid capacitance of V2b. Stray capacitance is minimised by the use of direct coupling between sections.

86. Signal grid tuned circuits are selected by SA5F and SA5B, as detailed in Tables 9 and 10. C36 is in series with C3 when SA is in position 3 (20Mc/s), thus reducing the swing of the variable capacitor over the range 20-27Mc/s.

87. Oscillator voltage is injected at the cathode of V2B, the anode load of which is L18, the primary of the first i.f.1 transformer, damped by R16.

88. L18 is connected to V2B anode by a screened cable, the outer braid of which connects the H.T. supply to the primary winding.

I.F.1 Amplifier, V3 and V4

89. The i.f.1 amplifier consists of two pentode stages with inter-stage coupling provided by T1, T2 and T3. The tuning range of the amplifier is 1-2Mc/s, within which range the output frequency of the first mixer lies.

Tuneable i.f. amplifiers present two problems:

(a) that of providing constant gain over the tuning range

(b) that of maintaining a constant passband over the tuning range.

90. The first problem is minimized by tuning the i.f. transformer primary windings to a frequency well below those covered by the tuning range, and by keeping the coupling factor low between the primary and secondary windings. Under these conditions the gain at the l.f. end of the tuning range is greater than that at the h.f. end. The addition of a small capacitor between the windings has the effect of increasing the transfer ratio more at h.f. than at l.f. so that by careful choice of capacitor value the gains at the ends of the tuning range can be made very nearly equal. The addition of the capacitor also helps to maintain the passband constant over the required range. Fig 15 shows part of the circuit of the i.f.1 amplifier, V4 and T3, which couples V4 to second mixer V5, being omitted from the diagram.

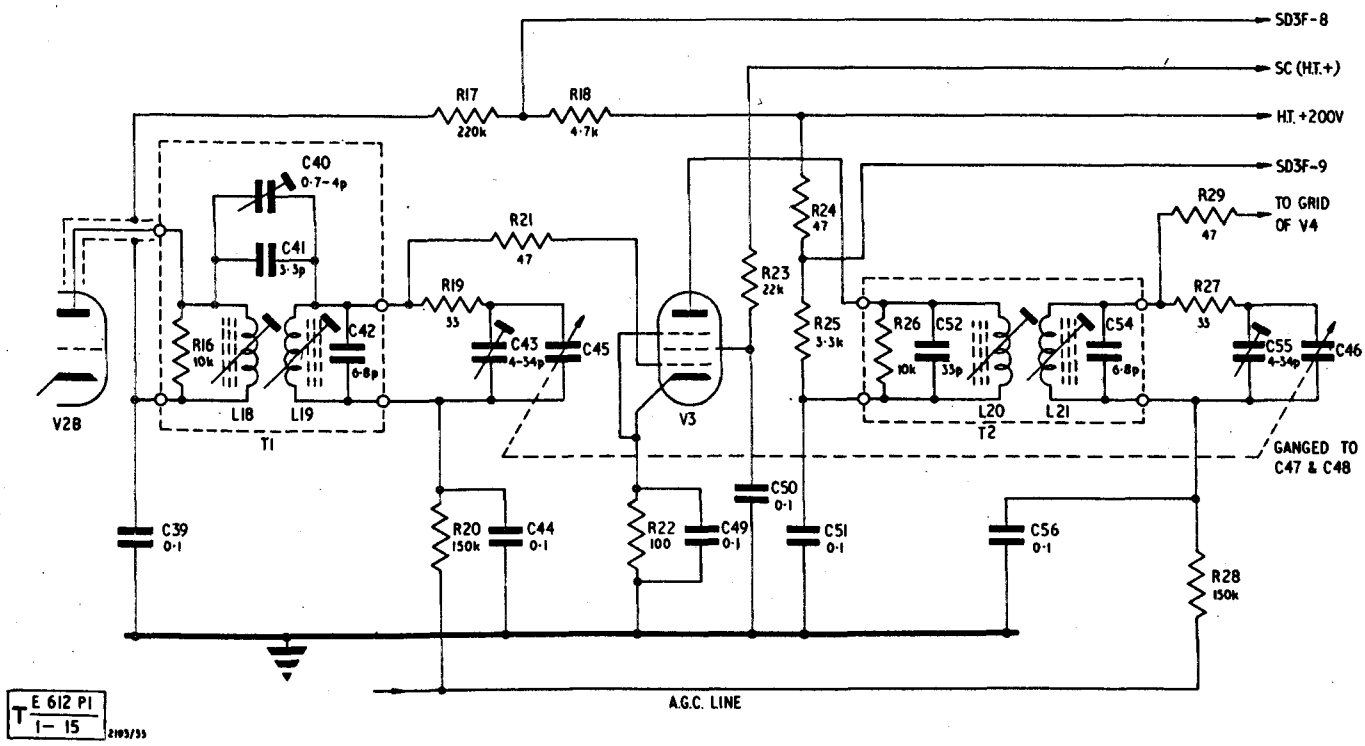

Fig 15 - First i.f.1 amplifier, circuit diagram

91. The primary windings of T1, T2 and T3 are tuned to 500kc/s and damped by 10kΩ resistors. Shunt capacitors across T2 and T3 primary windings are 33pF, but the self-capacitance of the screened cable connected across the primary winding is used in place of a parallel capacitor in the case of T1. The additional inter-winding coupling capacitor referred to in the previous paragraph is represented by C40 and C41.

92. All three transformer secondary windings are tuned between 1-2Mc/s by the ganged capacitor operated by the kc/s controls. Trimming is carried out by parallel connected 4-34pF capacitors. The 33Ω resistors in the secondary circuits are included to broaden the passband at the l.f. end of the tuning range.

93. A.G.C. is applied conventionally to V3 and V4 and in addition, the manual gain control bias is applied to the a.g.c. line. When the receiver desensitizing circuit is operated by the transmitter a fixed bias of approximately -40V replaces the manual gain control voltage. (See para 295 for gain control and desensitizing system details). There is no a.g.c. feed to T3 secondary so that the bottom end of this winding is earthed.

94. H.T. to the screen circuits of V3 and V4 is applied through SC which is a single wafer single pole eleven contact switch ganged to the s.f. tuning capacitors and so operated by the SF TUNING control. The switch is included to ensure that the s.f. circuits cannot be peaked on an image frequency. The screen supply is switched off by SC and the receiver thus muted when the signal circuits are tuned away from the correct frequency towards an image.

95. The valve screen circuits are connected to the pole contact of the switch wafer. H.T. is applied to one wafer contact only at a time, the positions of SA and SB determining the particular contact to which the supply is connected. Thus h.t. is fed to the screens over only a limited portion of the total physical swing of the ganged capacitor and the switching circuit is so arranged that the supply is connected only over the particular portion of the band in which the required signal lies.

96. When SA and SB are at positions 0, 3 or 0, 4, SC is inoperative and h.t. is supplied to the screens over the whole s.f. tuning band.

Second oscillator, V8 and V9

97. The second oscillator is a Franklin type. It is continuously variable over the range 1.1-1.2Mc/s. High mechanical stability has been achieved by rigid construction and the temperature coefficient of the oscillator is 10 parts in 10^6 per degree centigrade. The oscillator circuit, Fig 16, consists of a frequency determining l.c. circuit followed by a two stage r.c. amplifier.

98. The frequency determining circuit comprises L31 tuned by C48, C165, C166, C167, C168 and C169. C166 and C168 padding capacitors have a negative temperature coefficient. C167 is a Tempatrimmer, a miniature air dielectric temperature compensating capacitor. (See para 100 for details).

99. C 170 (5.6pF) loosely couples the l.c. circuit to the control grid of V8 which is triode connected. Positive feedback voltage is tapped off the decoupled

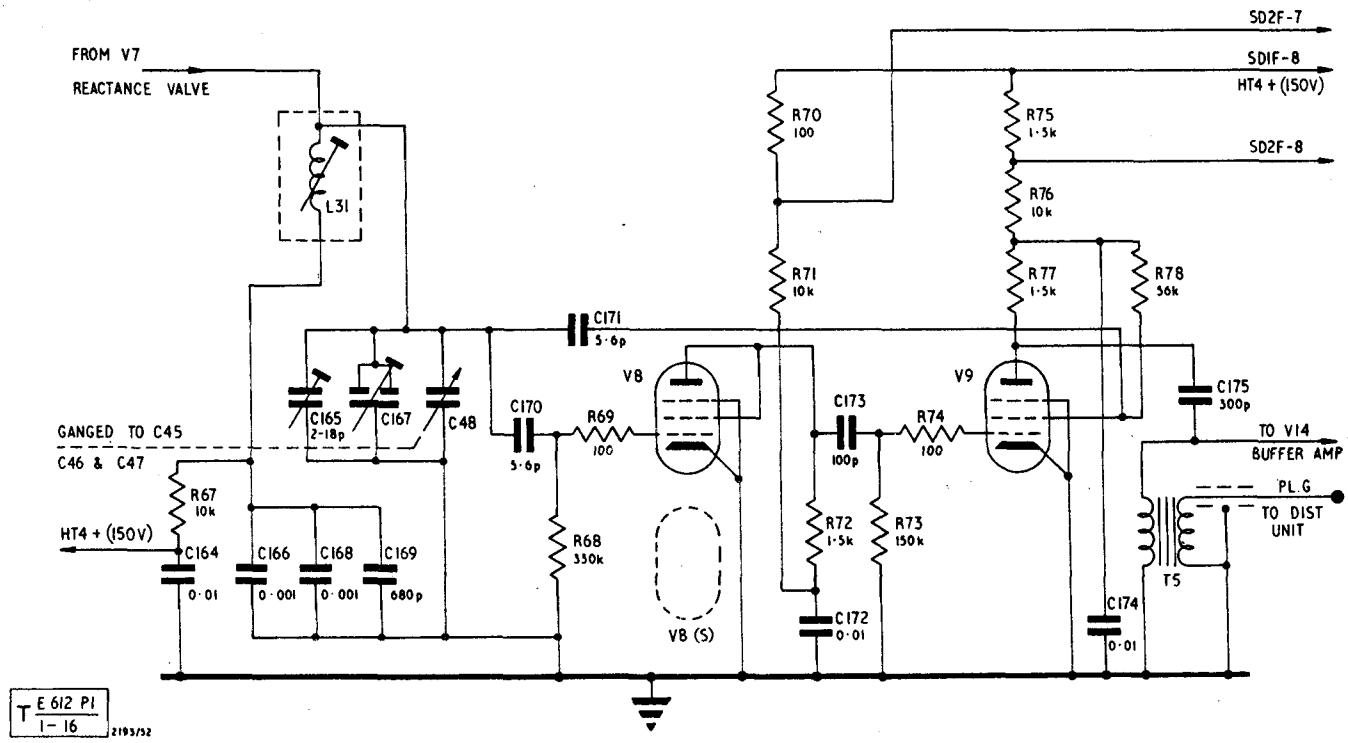

Fig 16 - Second oscillator, circuit diagram

screen of V9 and back coupled to the tuning circuit by C171. Oscillator output is taken from V9 anode and coupled to V14 and T5 by C175. T5 and spare valveholder V8(s) are used only when the receiver is in dual diversity.

C167, Tempatrimmer

100. C167 (Fig 17) is a miniature air dielectric capacitor which is continuously adjustable for temperature coefficients from +2000 through 0 to -2000 parts per million per degree centigrade over a temperature range of -40°C to +100°C. Nominal capacitance at room temperature is 6.5pF.

101. The U-shaped stator is fixed to one end of a bimetal strip, the other end of which is anchored to the ceramic base of the capacitor.

102. When the ambient temperature changes, the free end of the strip, and with it the stator, describes very approximately a section of an arc around the anchorage point. Over the short amount of travel involved, this may be regarded as a linear movement towards one or other of the sides of the capacitor (an upwards or downwards movement, referring to Fig 17).

103. The amount and direction by which the capacity changes with temperature depends upon the rotor position. Maximum change occurs when the curved part of the rotor

is pointing to one or other of the capacitor stator sides. If the rotor is positioned with its curved part pointing along the line of the bimetal strip, capacity change with stator movement is at minimum as increased area of plate mesh on one side is offset by a decrease of similar amount on the other side.

104. If the rotor is set as in Fig 17, the upward movement of the stator with temperature increase, reduces the plate mesh area. Conversely, when the temperature drops below ambient, the stator moves downward resulting in a capacity increase, i.e. a negative temperature coefficient.

105. The correct position of the rotor for normal working in the R234 is as illustrated in Fig 17.

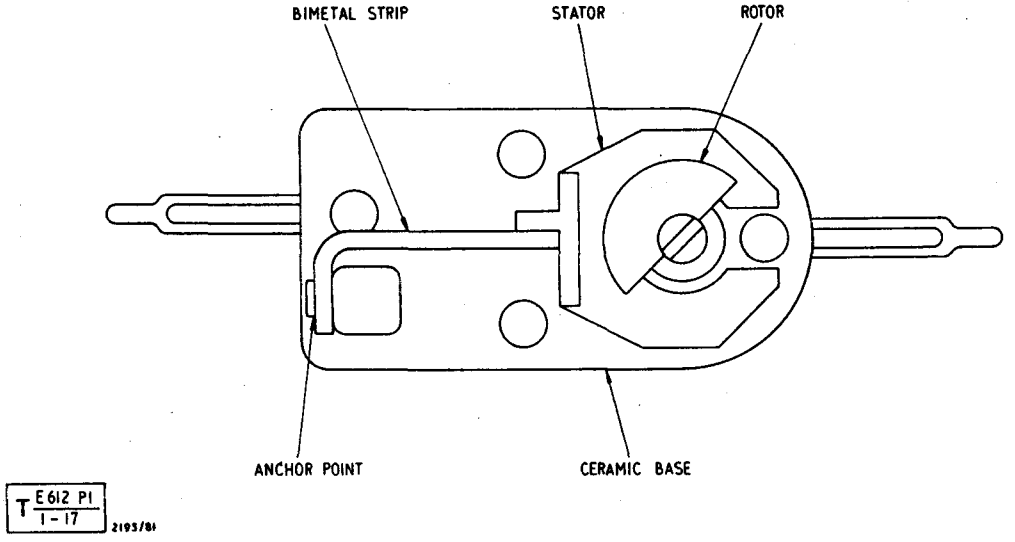

Fig 17 - Tempatrimmer capacitor, illustration

Reactance valve. V7

106. The purpose of the reactance valve circuit (Fig 18) is to enable the second oscillator frequency to be varied within narrow limits by the automatic frequency control voltage (d.c.) which is derived in either the s.s.b. unit (para 190) or the telegraph unit (para 276). The polarity of this voltage (with respect to earth) depends upon the direction of receiver off tune and its magnitude is proportional to the amount of receiver off-tune. (See EMER Tels A 013 for description of reactance valve).

107. V7 is a variable-μ r.f. pentode connected in such a way as to appear as a variable inductive reactance across the second oscillator frequency determining circuit.

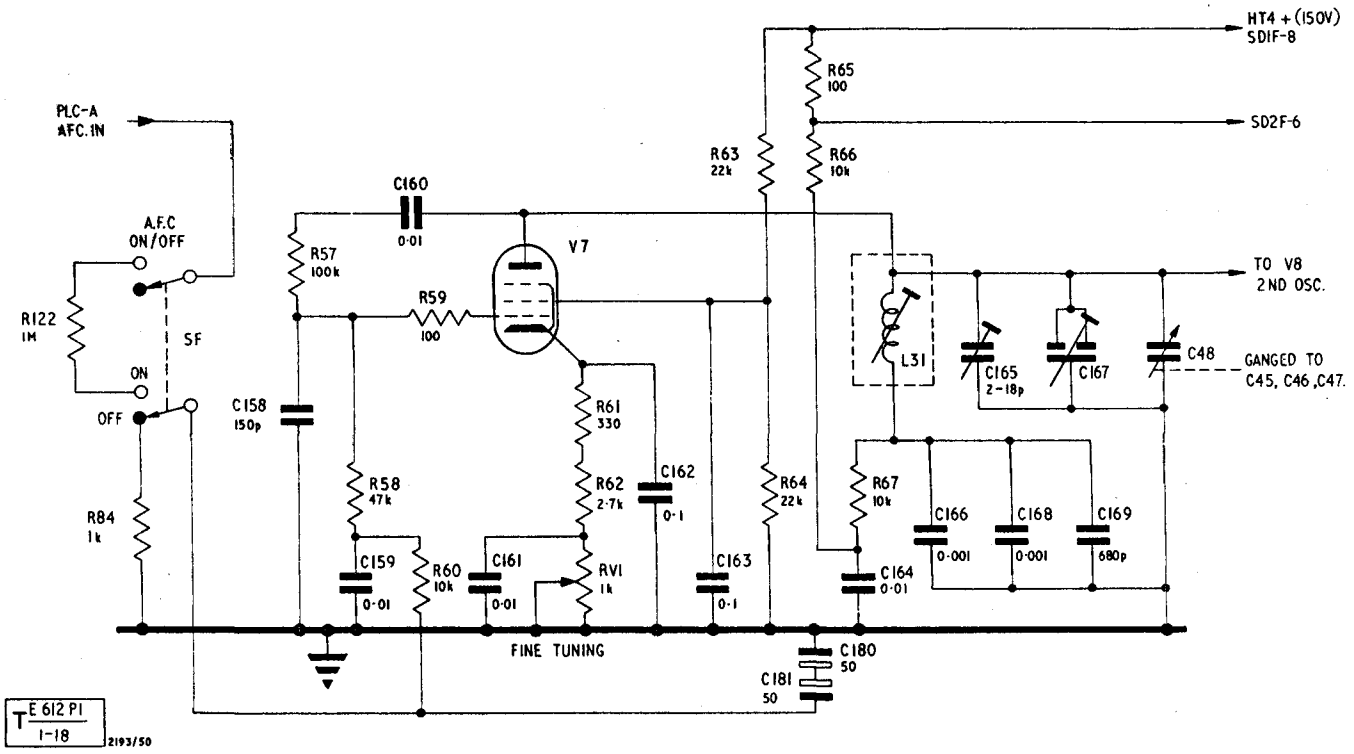

Fig 18 - A.F.C. reactance valve, circuit diagram

108. RF voltage is fed to V7 anode from the second oscillator and thence to the control grid after a 90° phase change by C158 and R57. C160 is acting purely as a d.c. blocking capacitor, its reactance being very small at the operating frequency, 1.1-2.1Mc/s.

109. The a.f.c. voltage is fed to the control grid as a grid bias, and variation of this voltage will change the apparent reactance of the valve thus varying the oscillator frequency above or below its nominal figure. Filtering of the control voltage is by C180, C181, R60 and C159. C180 and C181 are Tantalum capacitors connected back to back to form a non-polar high capacity reservoir.

110. Cathode bias is provided by series connected R61, R62 and RV1. The variable resistor is the front panel mounted FINE TUNING CONTROL which provides a second oscillator frequency variation of approximately 200c/s.

111. Use of a.f.c. reduces frequency drift up to 3kc/s to less than 20c/s on telephony and to less than 10% of total shift on f.s.k.

Second oscillator buffer amplifier, V14

112. V14 is used in a buffer circuit, Fig 19, to isolate the oscillator stage and to amplify its output to the level required for injection into the second mixer. T5 is included for use when the receiver is working in dual diversity.

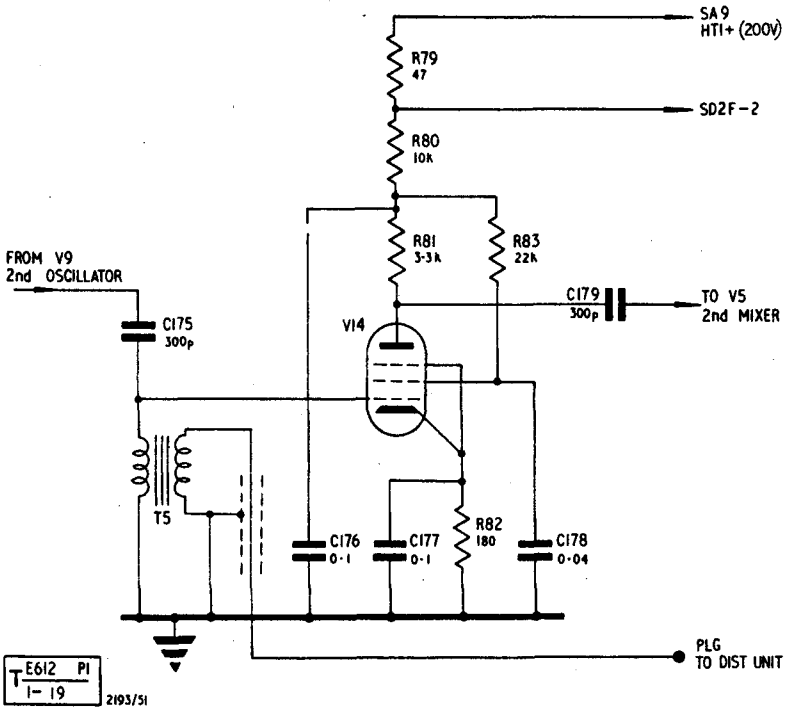

Fig 19 - Second oscillator buffer amplifier, circuit diagram

Second mixer, V5

113. The second mixer stage uses a heptode. The circuit is shown in Fig 20.

114. The variable frequency i.f.1 signal is injected at g3 of V5 from T3 secondary winding, which is tuned between 1-2Mc/s by C47.

115. The second oscillator signal between 1.1 and 2.1Mc/s from V14 is fed to g1 of V5 via C179. A test point, normally shorted by a removable link, is provided between R37/R39 to enable grid current to be measured. C64 then acts as a decoupling capacitor across the microammeter.

116. The 100kc/s difference frequency which is the second i.f., is developed across V5 anode load, L24, C67 and R42, and coupled from T4 secondary to a delta pad by C68. Outputs from the pad are fed to the s.s.b. unit for use when receiving telephony and to the telegraph unit for use when working c.w. or f.s.k.

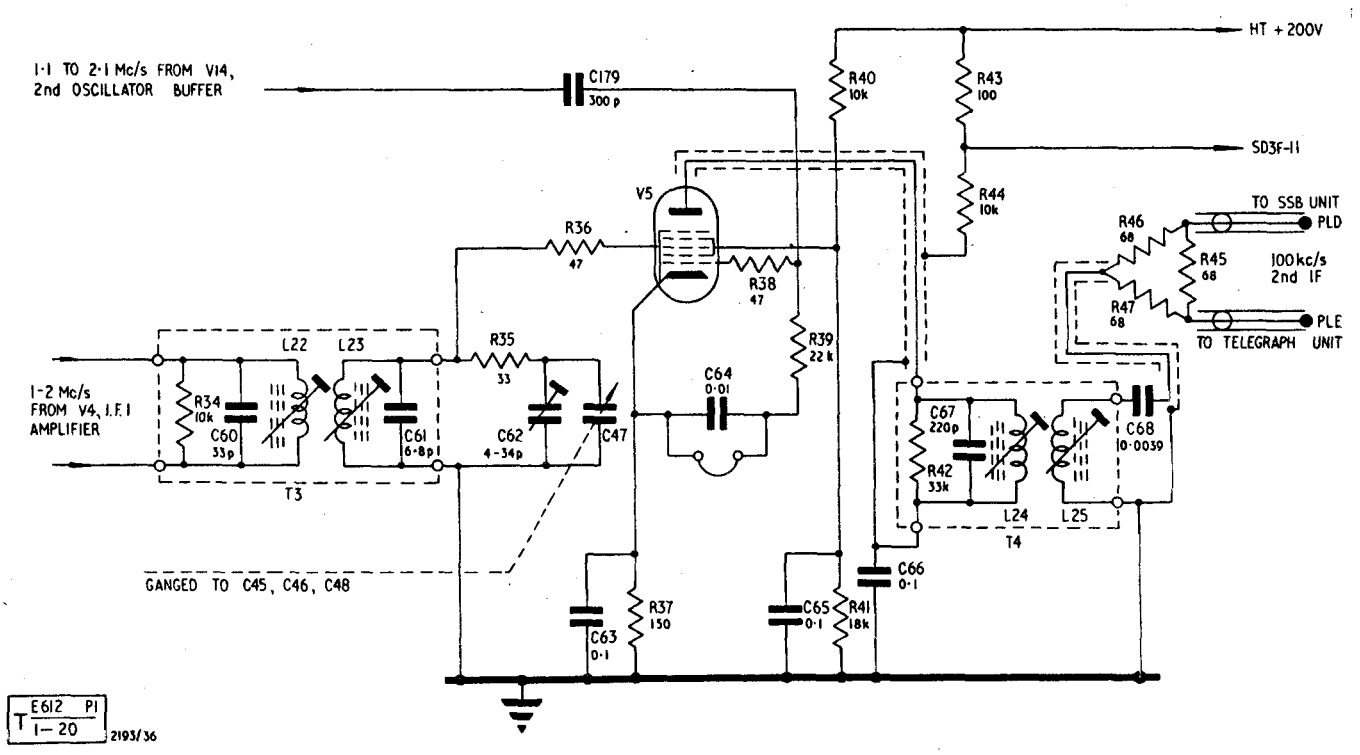

Fig 20 - Second mixer, circuit diagram

Crystal calibrator V10, V11, V12 and V13

General

117. The crystal calibrator generates signals at intervals of 100kc/s or 10kc/s throughout the tuning range of the receiver. The frequency calibration can therefore be checked at any 100kc/s or 10kc/s point in the range 2.1-27Mc/s and corrected as necessary by adjustment of the movable cursor of the fine kc/s scale by means of the SET ZERO control.

118. The calibrator also provides a 100kc/s signal which may be used as a local carrier or which is fed to the telegraph unit for use as a tuning signal when the system switch is at CAL.

119. Four stages are used to generate the carrier and calibration signals. These are:

(a) 100kc/s crystal oscillator (V10)

(b) limiter (V11)

(c) 100kc/s multivibrator (V12)

(d) 1Ckc/s multivibrator (V13)

Crystal oscillator V10 and limiter V11

120. Fig 21 shows the circuit of V10 and V11.

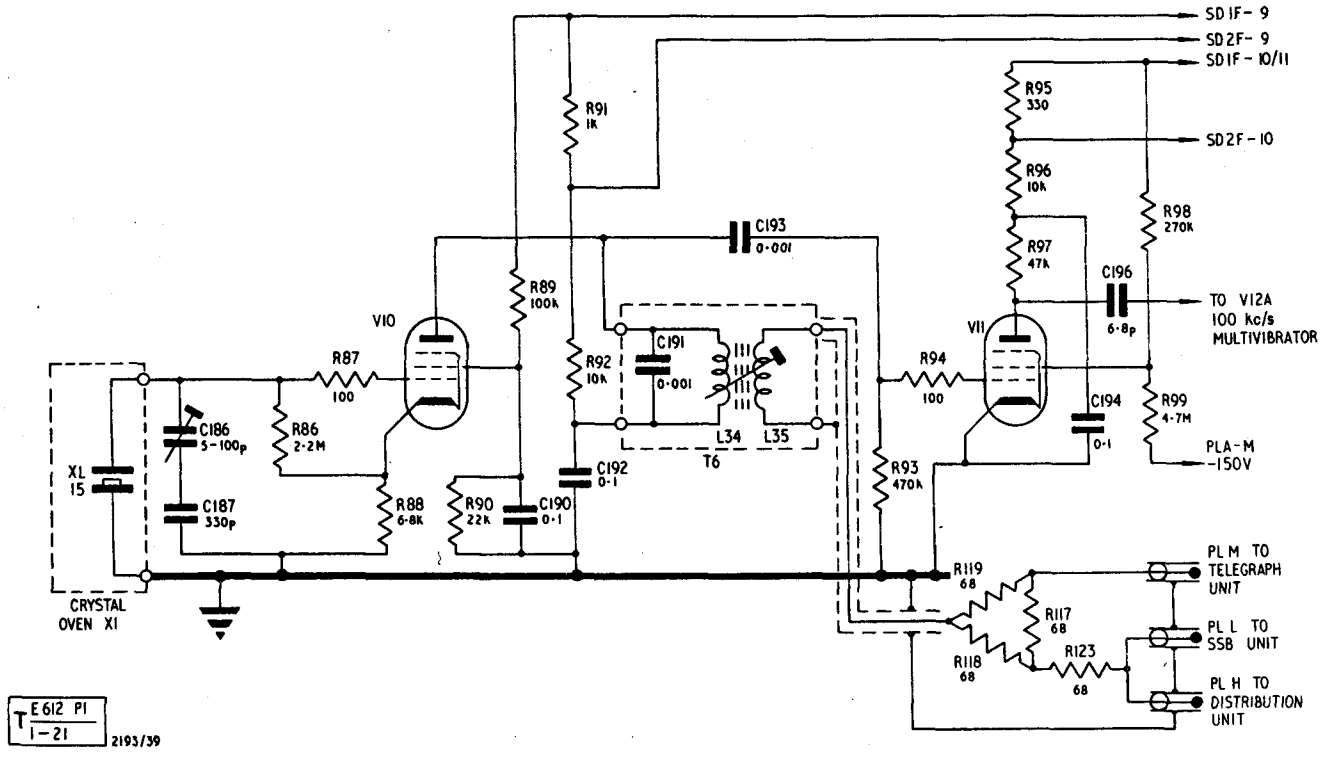

Fig 21 - Crystal oscillator and limiter, circuit diagram

121. The 100kc/s oscillator crystal, XL15, is contained in a thermostatically controlled oven. Crystal frequency can be adjusted to the required accuracy of 100kc/s ±0.5c/s by C186.

122. L34 and C191 form the oscillator anode circuit which is inductively coupled to a splitter pad comprising R117, R118, R119 and R123. The pad distributes the sine wave output as follows:

(a) via PLL to the s.s.b. unit for use as a locally generated carrier.

(b) via PLM to the third mixer, V21A, in the telegraph unit to act as a tuning signal during frequency calibration.

(c) via PLH to the distribution unit for use when the receiver is acting as Master in a dual diversity station.

123. In addition, the oscillator output is coupled to limiter V11, the output from which triggers asymmetrical multivibrator V12.

100kc/s multivibrator, V12

124. The circuit is shown in Fig 22. In its stable state under no signal conditions V12A is cut off, its grid being -150V with respect to cathode (earth), and V12B is conducting. Upon the arrival of a triggering pulse from V11, V12B tends towards cut-off, and its anode potential thus starts to rise. C199 and R105 couple this positive swing to the grid of V12A, which then starts to conduct. V12A anode potential falls and the negative swing, coupled by C197, cuts off V12B. The charge on C197 leaks away through R104 and the grid potential of V12B rises exponentially until the valve again conducts, and its anode potential starts to fall. V12A cuts off and this stable state exists until the onset of the following trigger pulse.

125. The circuit constants are such that a spiky output waveform is obtained since this provides better calibration signals than the more normal multivibrator square wave output.

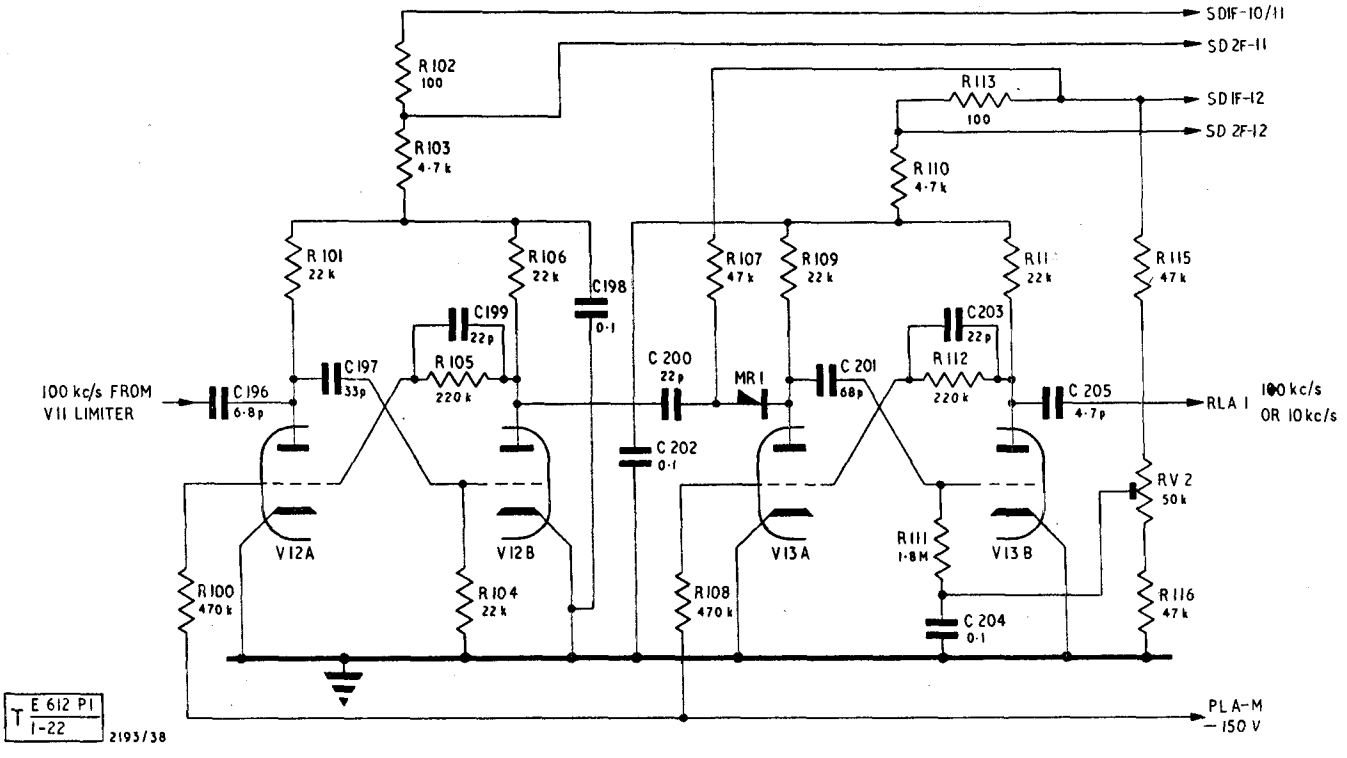

Fig 22 - Multivibrators, circuit diagram

10kc/s multivibrator, V13

126. The circuit of the 10kc/s multivibrator stage is similar to that used for the 100kc/s multivibrator except for component value differences and the inclusion of a frequency control (RV2).

127. V12B output is coupled to V13A anode by C200 and MR1, which is included to shape the trigger pulse from V12. R107 biases the diode.

128. RV2 forms part of a potentiometer chain across the H.T. supply, and adjusts the repetition frequency of the stage.

129. The calibrator output at V13B anode is coupled to the receiver input circuit by C205 and RLA. When switched to CAL100, V13 is inoperative and V12 output is coupled to C205 by V13 inter-electrode and stray capacities.

H.T.5 switching and routing

130. A simplified circuit of the HT5 supply switching and routing for the calibrator valves is given in Fig 23.

131. H.T. switching is carried out by the system switch (SA) on the telegraph unit, by the reconditioned/local carrier switch (SB) in the s.s.b. unit and by the MASTER/SLAVE switch SG on the s.f. and i.f.1 unit.

132. On the D.S.B., S.S.B. and I.S.B. positions of SA, V10 can be used as a local carrier generator by switching SB, s.s.b. unit, to LOCAL. V11, V12 and V13 are then inoperative and load compensating resistors R188-R193 inclusive are switched across the HT5 rails. When reconditioning the transmitted carrier with SB at REC, all calibrator valves are inoperative and resistors R188-R194 inclusive are shunted across the HT5 supply.

133. When SA is at CAL 100, V10, V11 and V12 are operating and R188, R189 and R190 are switched across the supply.

134. When SA is at CAL 10, all the calibrator valves are functioning and there is no resistive loading switched across HT5.

135. On C.W. and F.S.K. positions of SA, all the calibrator valves are inoperative and HT5 supply is loaded by R188-R194 inclusive.

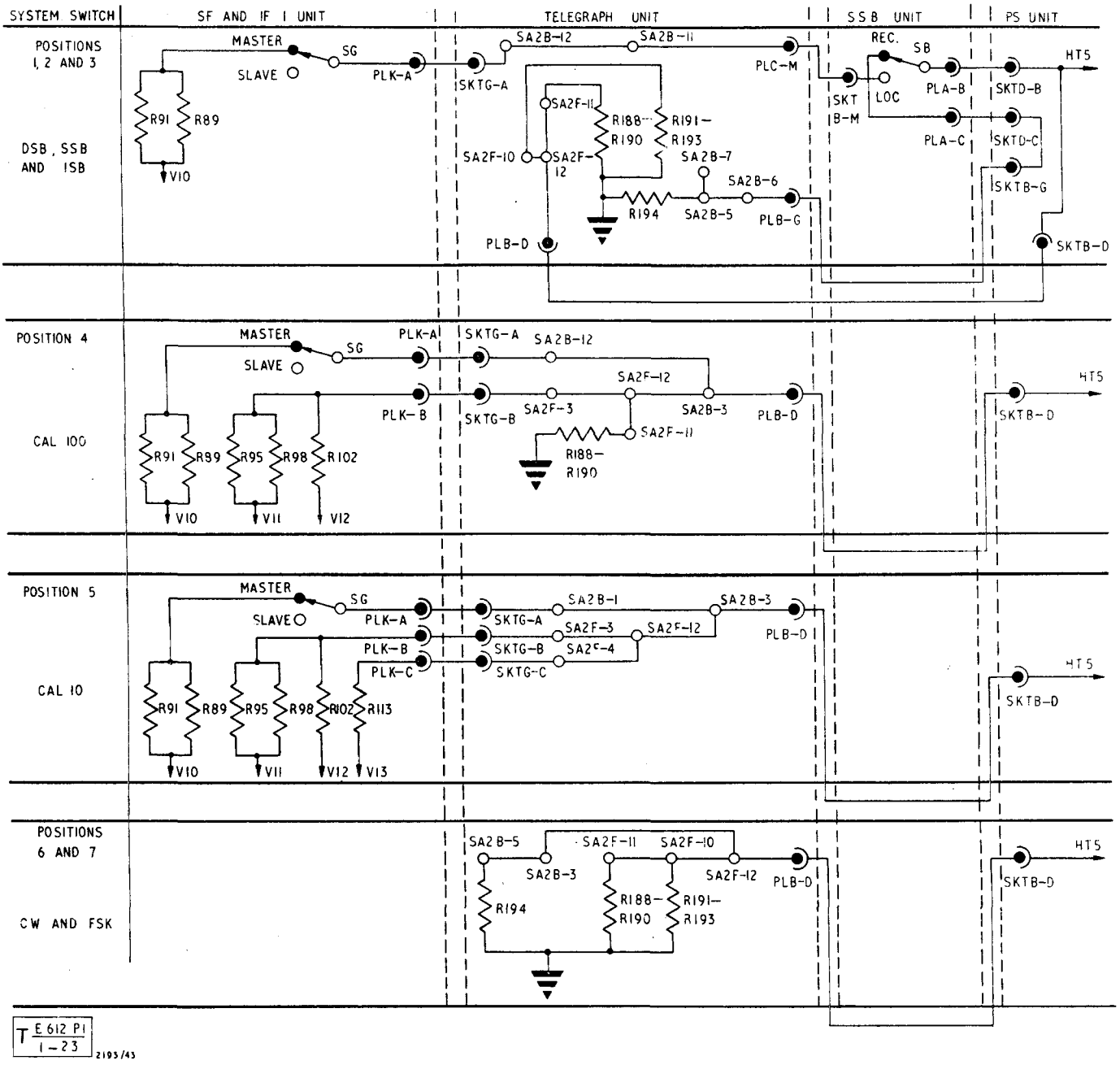

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Fig 23 - H.T.5 switching and routing, simplified circuit diagram

Crystal oven

Construction

136. Fig 24 illustrates the components of the crystal oven. It comprises the following:-

(a) Base with an octal plug on the underside and a B7G socket and three separate contacts mounted on the topside.

(b) Oven block in two halves.

(c) Heater.

(d) Thermostat.

(e) Glass enclosed 100kc/s crystal with B7G base.

(f) Evacuated glass envelope.

(g) Aluminium outer cover.

(h) Spring loaded bayonet fitting top cover.

137. Connections are taken from the octal base to the B7G socket and to the three separate contact pins on the topside of the base.

138. The oven block is constructed of nickel plated brass in two halves, screwed together but electrically insulated from each other. The heater is mounted in the lower part whilst the thermostat is held between the two halves, making contact with both.

139. The crystal is enclosed in the oven block and the three pins on the base mate with terminations in the block to convey the supplies to it and to the heater.

140. The evacuated glass envelope encloses the oven block and rests on a PVC moulding fitted over the topside of the base. The whole is contained in the outer case with the octal plug protruding through the bottom. The top cover retains the envelope in position. The complete oven is held in the octal socket on the calibrator sub-chassis by a spring cradle.

Control and heater circuits

141. Fig 25 shows the complete oven circuit.

142. The thermostat contacts are in series with the negative side of the relay energizing supply and remain open until the oven reaches its operating temperature of 72°C-75°C.

143. With the thermostat contacts open, RLB is not energized and the 6.3V a.c. supply is connected to the heater and to ILP1, the front panel OVEN lamp. When the oven reaches operating temperature, the thermostat contacts close and RLB is energized thus breaking the heater supply contacts. The oven cools until the thermostat contacts again open, and the cycle is repeated.

144. Filters included in both supply lines to the oven ensure that switching interference is reduced to a minimum.

145. The heater on/off cycle, as indicated by ILP1, normally commences within 30 minutes of switching on, but some two hours are required for temperature stabilization. Correct operation is indicated by regular cycling of the indicator lamp.

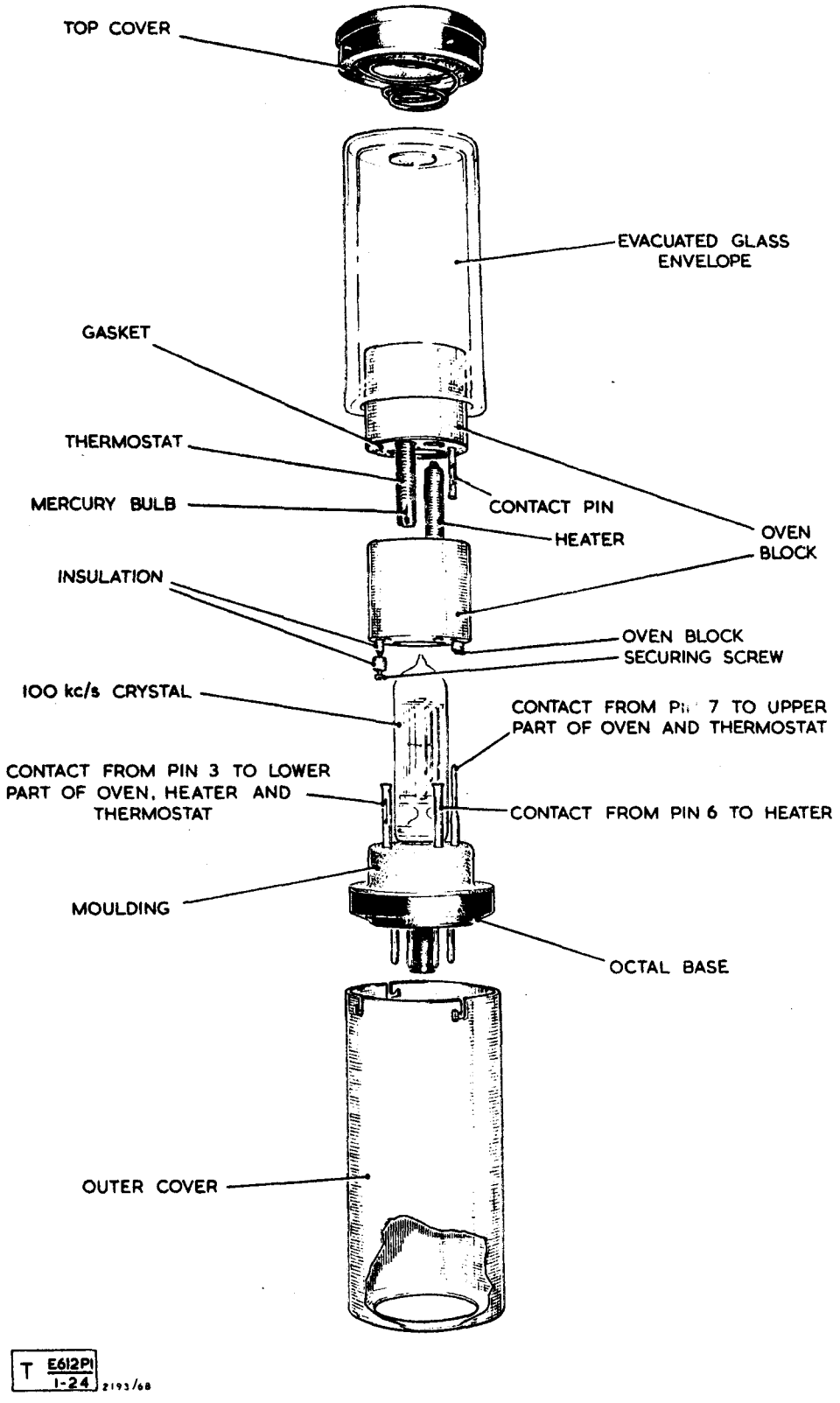

Fig 24 - Crystal oven, construction and component parts, illustration

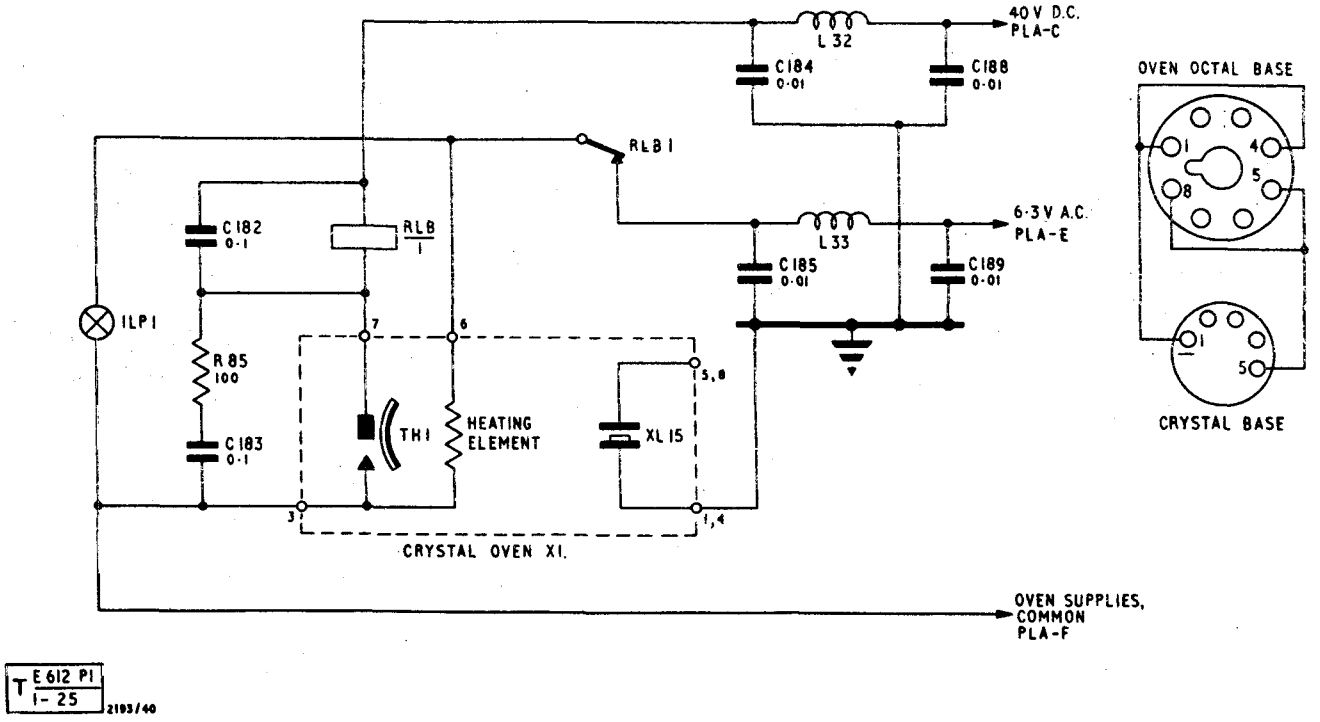

Fig 25 - Crystal oven heater and control, circuit diagram

Monitoring facilities

146. Current monitoring resistors are included in all valve anode circuits to allow anode currents to be checked. SE and SD switch M1 across the monitoring resistor of the selected valve. Provision is also made for checking the drive to V15 buffer/multiplier by grid current monitoring. SE and SD switch M1 across R53 for this check.

Supplies

H.T.

147. V7, V8 and V9 are supplied by HT4 +150V stabilized supply. HT5 +150V stabilized supply feeds V10, V11, V12 and V13, whilst the remainder of the valves receive H.T. from the HT1 +200V line.

L.T.

148. All valve heaters, with the exception of V7, V8 and V13, are parallel fed from LT2, 6.3V a.c. supply. ILP2-ILP9 are illuminated by the same supply.

149. Filtering for the supply to V1 heater is provided by L36 and C206.

150. V2 and V12 have centre tapped heaters and the two halves are connected in parallel across LT2. L37 and C207 filter the supply to V2.

151. V3, V4 and V5 supply is filtered by L41 and C213.

152. The bases of V6 and V15 are contained in a screened compartment and l.t. is supplied via feedthrough capacitor C208. C208, C209, L38 and L39 ensure that stray radiation at V6 or V15 operating frequency does not take place from the heater wiring outside the oscillator compartment. Further precautions against stray radiation are included, L40, L42, C210, C212 and C214 being the components concerned.

153. The supply for V7, V8 and V13 is 12.6V d.c. stabilized from Power Supply Unit, type 5441A. V7 and V8 are series connected but have different current ratings. R121 is in parallel with V7 heater to equalise the voltage drops across the heaters of the two valves.

S.S.B. UNIT TYPE 5415A
(Fig 2508-2514)

General

154. The special circuits required for sideband reception are contained in the s.s.b. unit. The same circuits are used for d.s.b. reception. The unit also accommodates the circuits for telephony, a.g.c., a.f.c. and tuning indication.

155. Major compcnents are mounted on the topside of the chassis, whilst the smaller items are mounted on tagboards secured to the underside. The chassis can be tipped up and locked when withdrawn.

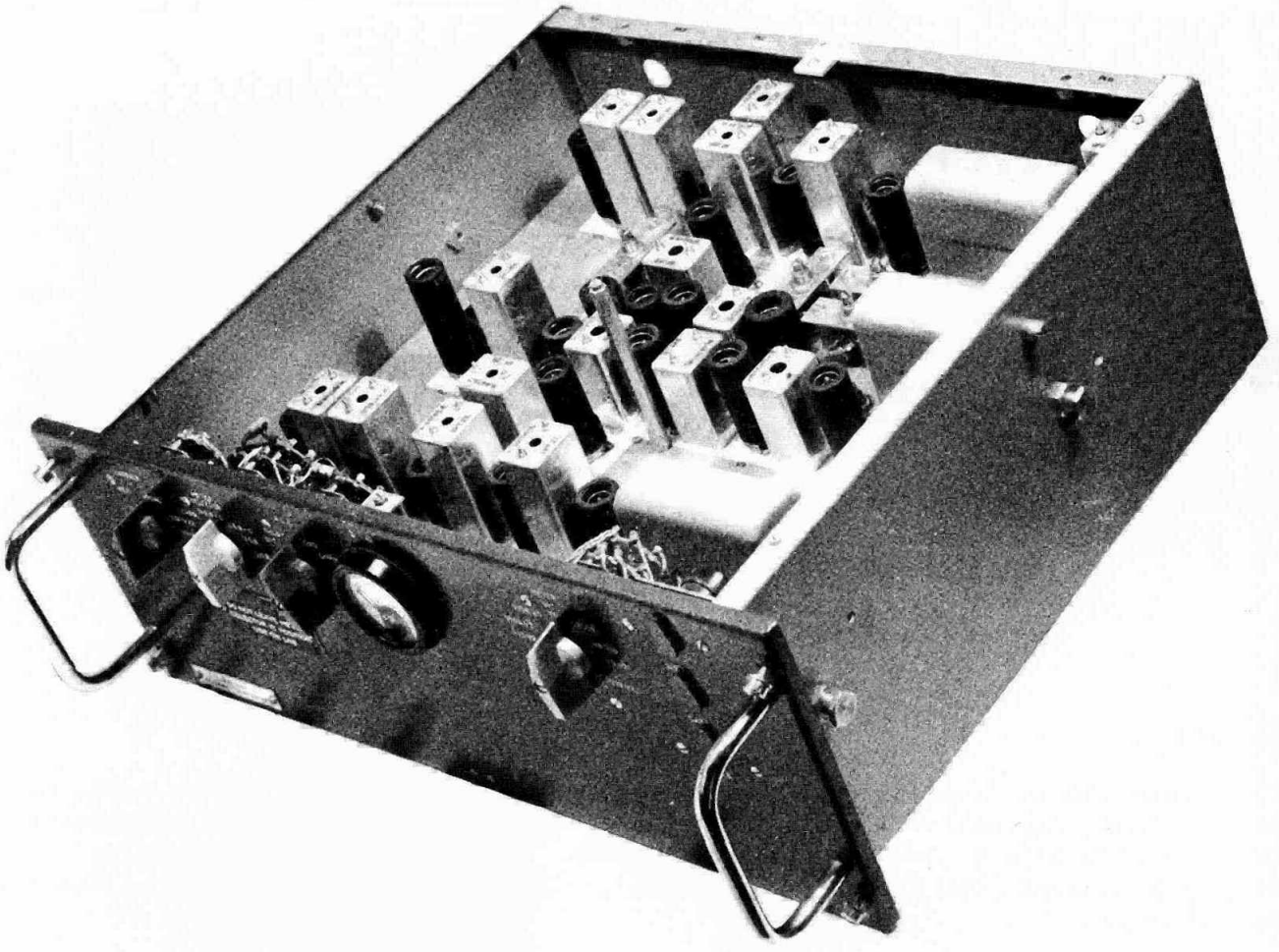

Fig 26 - S.S.B. unit, general view

156. The general view of the unit, Fig 26, shows the u.s.b. chain mounted from right to left immediately behind the front panel. The l.s.b. chain is at the rear of the chassis whilst the carrier chain occupies the chassis centre together with a.g.c. and a.f.c. components.

157. Front panel control functions are detailed in Table 2. Fig 27 is a block diagram of the unit.

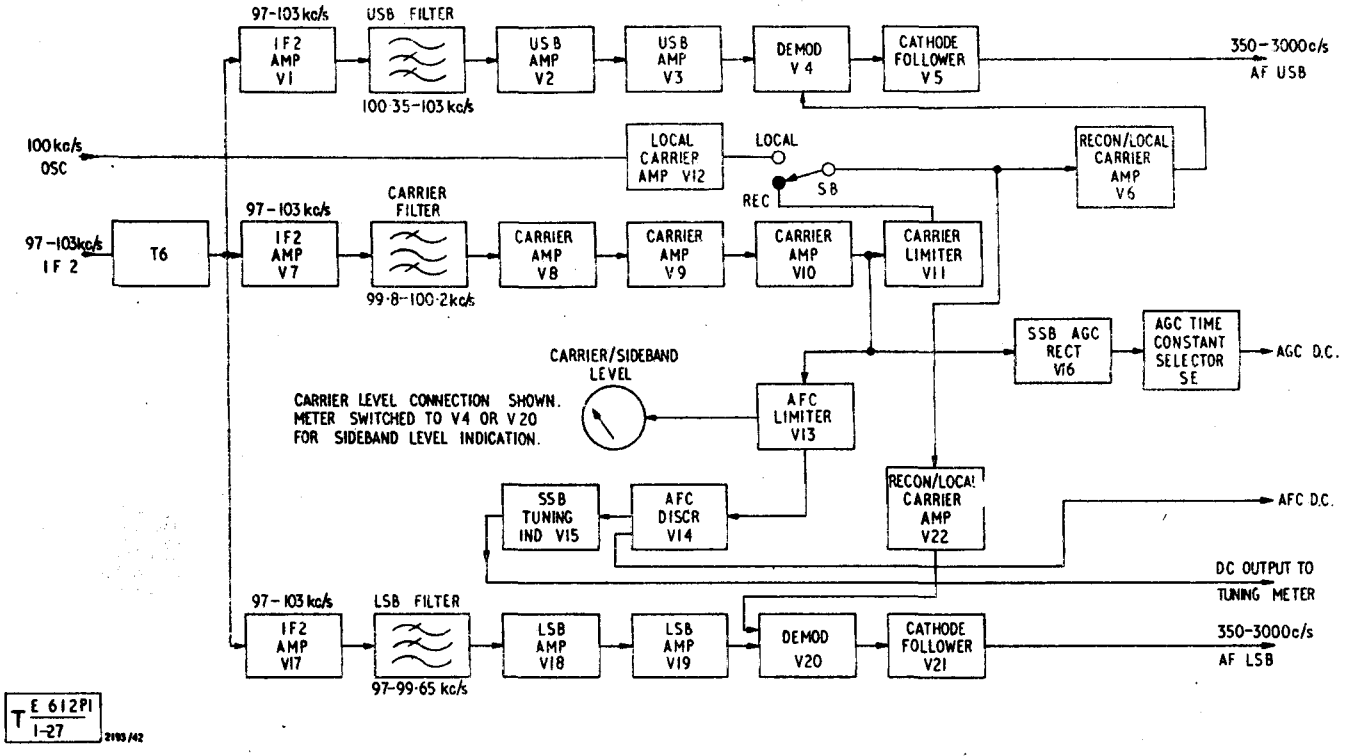

Fig 27 - S.S.B. unit, block diagram

Filters

158. Three two section half lattice type filters are used in the s.s.b. unit, one in each chain to separate the upper sideband, lower sideband and carrier components from the composite 100kc/s second i.f. signal. They operate as inter-valve couplings between 18kΩ terminations. Fig 2510 shows the basic circuit of the sideband filters.

159. All filters are housed in hermetically sealed containers which are filled with dry nitrogen for greater stability of performance. It is not possible to carry out any adjustments or repairs to the filters and no attempt must be made to open the containers. Any filter which has been proved faulty must be disposed of in accordance with EMER Tels A 801.

160. Table 14 shows details of filter performance. Fig 2512 and 2513 show the theoretical curves.

Table 14 - S.S.B. unit filter characteristics

Filter	Centre frequency kc/s	3dB bandwidth c/s	Passband kc/s	Insertion loss dB
U.S.B.	101.675	2650	100.35-103	8
Carrier	100	400	99.8-100.2	9
L.S.B.	99.325	2650	97-99.65	8

161. The 400c/s bandwidth of the carrier filter is greater than that normally encountered in commercial s.s.b. practice in order that any tuning error due to carrier or receiver oscillator drift, will not normally be sufficient to remove the carrier outside the filter passband. This assists in re-establishing communication rapidly after prolonged radio silence during which time the a.f.c. system will have been inoperative.

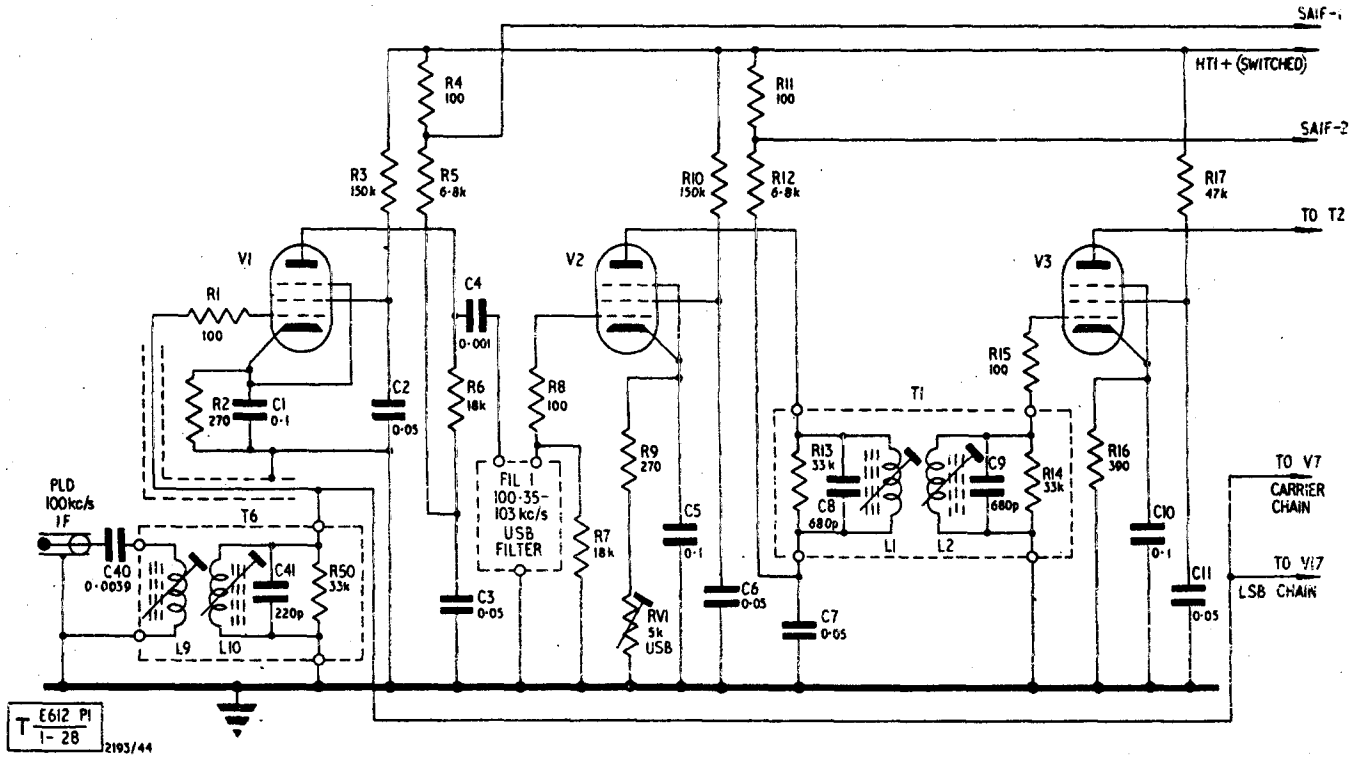

Fig 28 - U.S.B. amplifier, circuit diagram

Input circuit

162. The composite 100kc/s second i.f. signal containing upper and lower sideband and carrier components, enters the s.s.b. unit from the s.f. and i.f.1 unit at PLD. The signal is applied to the input step-up transformer T6, the secondary of which feeds the u.s.b., l.s.b. and carrier chains.

U.S.B. chain V1-V5

163. The circuit of the u.s.b. chain is shown in Fig 28 and 29.

164. The composite second i.f. signal from T6 is amplified by V1 and then applied to the u.s.b. filter. The u.s.b. signal, is amplified by V2, transformer coupled to V3, further amplified and then transformer coupled into the demodulator, V4.

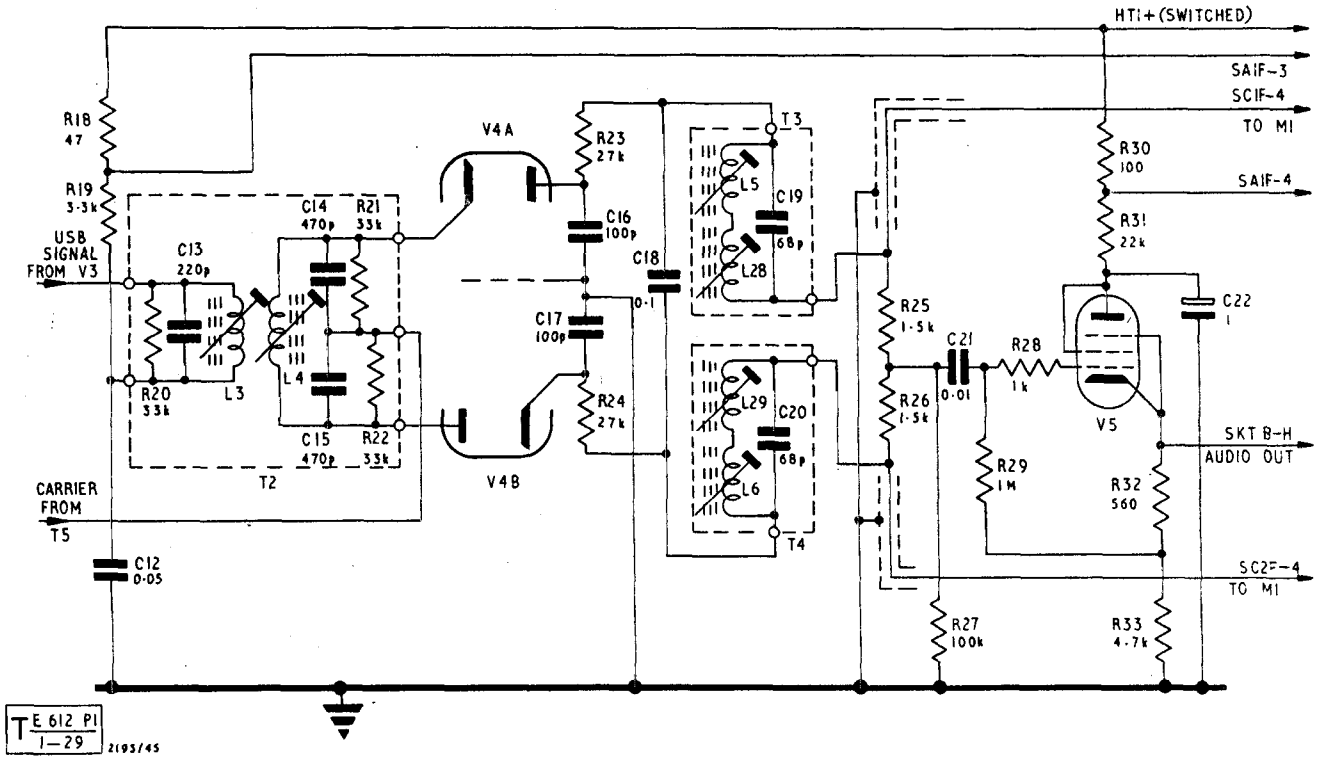

Fig 29 - U.S.B. demodulator and cathode follower, circuit diagram

165. The i.f. transformers are designed to have a flat response over the filter passband so that the overall response of the chain is primarily determined by the filter characteristics.

166. RV1 is a front panel pre-set control, identified U.S.B., used to set the u.s.b. signal level at the demodulator.

167. V4A and V4B are fed with a balanced sideband voltage from T2 secondary and with an unbalanced carrier voltage from reconditioned/local carrier amplifier V6, via T5.

168. In the absence of a sideband signal, equal and opposite voltages are produced at V4A cathode and V4B anode by the carrier, and equal and opposite voltages are developed across load resistors R24, R26 and R23, R25. The resultant voltage at their centre point with respect to earth, the voltage developed across R27, is therefore zero.

169. A sideband signal results in anti-phase voltages at the two diodes, so that when carrier and sideband voltages are in phase at V4A, they are anti-phase at V4B.

170. The voltage at V4B cathode follows the positive portion of the envelope of the i.f. signal whilst V4A anode voltage follows the negative half.

171. When carrier and sideband voltages are in phase at V4B anode, there is simultaneously an increase in the positive potential at the V4B end of the diode load, and a decrease in the negative potential at the V4A end. The potential at the centre point of the loads therefore becomes positive by the amount of the change, that is by an amount equal to the peak value of the sideband voltage applied to either diode.

172. The level of the carrier voltage is set to 20dB above peak sideband level at the diodes, and with this large ratio of carrier/sideband levels the combined signal is approximately sinusoidal.

173. Since the demodulator is balanced, even order distortion products are cancelled and the a.f. output, the frequency difference between sideband and carrier, approximates very closely to the original signal.

174. T3 and T4 and associated capacitors form rejector circuits tuned to 100kc/s. They are in series with the diode loads and minimize the residual level of carrier voltage present in the demodulator output.

175. The a.f. signal appearing across R27 is coupled to cathode follower V5 by C21. V5 is a triode connected pentode with R32 and R33 forming the cathode load. To provide the correct bias level, grid leak R29 is returned to the junction of R32/R33. C22 ensures that the anode and screen are at earth potential with respect to a.f.

176. The low impedance audio output is fed to the u.s.b. line amplifier in the telegraph unit.

L.S.B. chain, V17-V21

177. The circuit of the l.s.b. chain is similar to that of the u.s.b. circuit just described. T13 and T14 are however tuned to suit the different passband, and the L.S.B. front panel pre-set control for setting the sideband signal level at the demodulator is RV6.

Carrier chain, V7-V12

Reconditioned carrier circuits

178. The composite second i.f. signal from T6 is amplified by V7 and then applied to the carrier filter. Fig 30 and 31 show the circuit of the chain.

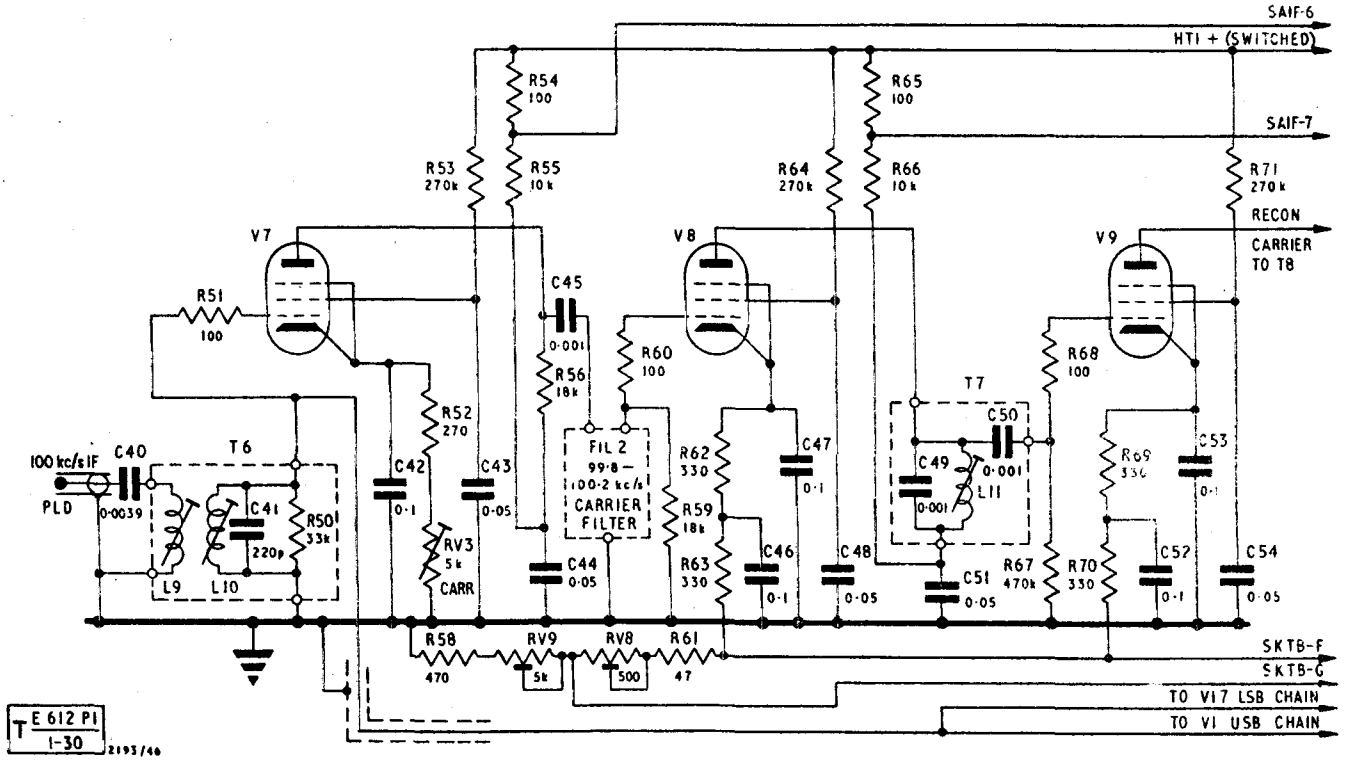

Fig 30 - Reconditioned carrier amplifier and gain switching, circuit diagram

179. The carrier component is amplified by V8, V9 and V10 carrier amplifiers and then fed to V13, a.f.c. limiter, by C69, and to V16, a.g.c. rectifier, by C83. V10 output is also applied to V11 limiter which has a common anode load, L16, with V12, local carrier amplifier.

180. With the CARRIER selector switch SF at REC, V11 is functioning and V12 is inoperative, h.t. being removed from its screen which is returned to -200V by R86. V11 constant amplitude output is taken to V6 and V22, the u.s.b. and l.s.b. local/reconditioned carrier amplifiers.

181. During s.s.b. transmission, the pilot carrier is radiated at a level of -13dB with respect to peak sideband level, and at -23dB during i.s.b. transmission.

182. An automatic gain adjusting circuit is incorporated in the carrier chain to ensure that the carrier is injected into the demodulators at the correct level (20dB above peak sideband level) on all telephony reception modes without the necessity of action by the operator. SA3B, system switch, telegraph unit and R58, R61, RV3, RV8 and RV9 in the s.s.b. unit are used to make the adjustments. See Fig 32 for a simplified circuit of gain switching.

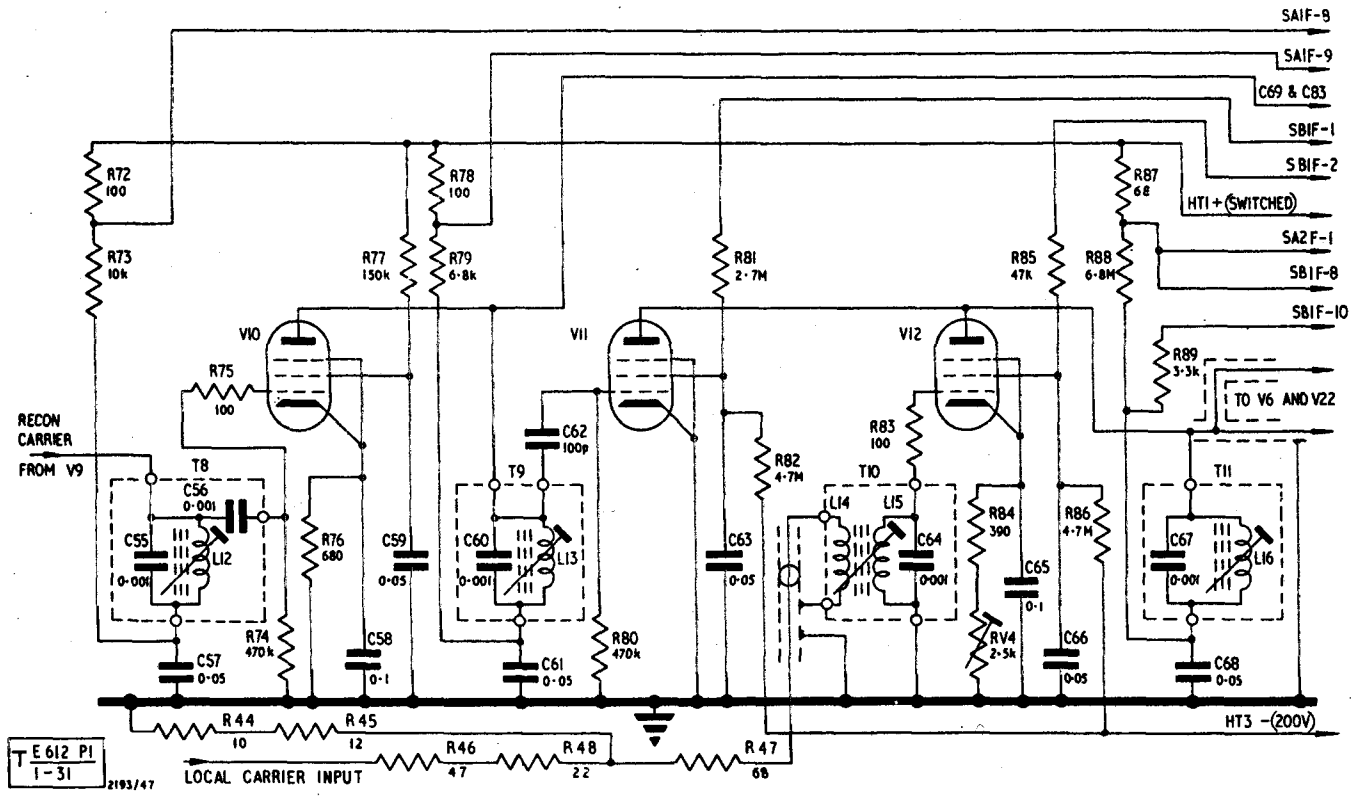

Fig 31 - Reconditioned carrier amplifier and local carrier amplifier, circuit diagram

183. On I.S.B. the gain of the carrier chain is controlled by V7 cathode bias control RV3 (CARR, front panel). When switched to s.s.b. R61 and RV8 are additionally in circuit and RV8 is adjusted to give the required gain reduction. On d.s.b. when sideband power is only a fraction of carrier power, R58 and RV9 are introduced into V8/V9 cathode circuit and RV9 is adjusted for further gain reduction. Thus by setting up RV3, RV8 and RV9 with the appropriate input level for the system in use, the carrier level at the demodulator is automatically correct on all telephony positions of the system switch.

Local carrier circuits

184. Under certain reception conditions when the pilot carrier fades badly, the use of a reconditioned carrier can cause considerable distortion of the signal. To overcome this difficulty a local carrier facility is incorporated whereby the output from the 100kc/s crystal oscillator in the calibrator is amplified and applied to the demodulator at the correct level in place of the reconditioned pilot.

185. When the system switch (SA, telegraph unit) is set to D.S.B., S.S.B. or I.S.B. and the CARRIER switch SB is set to LOCAL h.t.5 for V10 crystal oscillator in the s.f. and i.f.1 unit is switched on. SB also switches on h.t.1 for the screen of V12, local carrier amplifier, at the same time removing the h.t. supply from V11 which

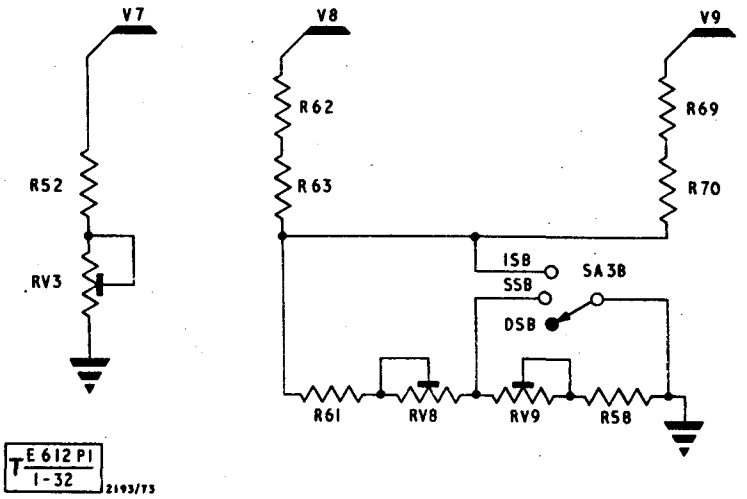

Fig 32 - Reconditioned carrier amplifier, gain switching, simplified circuit diagram

is then cut off, its screen being returned to -200V.

186. The signal from the oscillator enters the s.s.b. unit at PLC and is attenuated by a T network comprising R44-R48. It is then fed, via T10, to V12 which amplifies it to a suitable level for coupling to reconditioned/local carrier amplifiers V6 and V22. RV4 in V12 cathode circuit controls stage gain and is the local carrier gain control.

U.S.B. reconditioned/local carrier amplifier, V6

187. V6 receives and amplifies the output from either V12 or V11 depending upon whether local or reconditioned carrier is being used. V6 circuit is given in Fig 33.

188. Output from the amplifier is transformer coupled by T5 to the u.s.b. demodulator. RV2 allows variation of cathode bias and is the u.s.b. carrier gain control.

L.S.B. reconditioned/local carrier amplifier, V22

189. The circuit of V22 is identical to that of V6. The coupling transformer is T17 and RV7 is the l.s.b. carrier gain control.

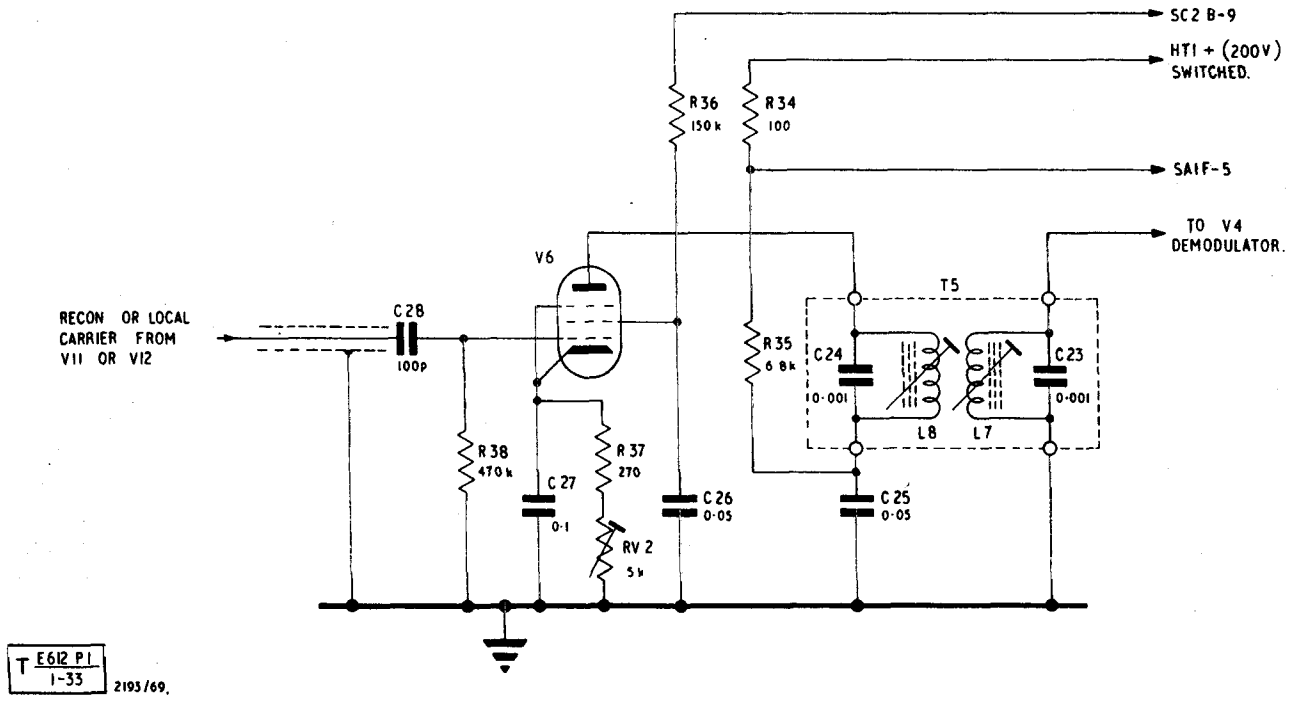

Fig 33 - U.S.B. local/reconditioned carrier amplifier, circuit diagram

A.F.C. system

General

190. The a.f.c. system employs a carrier driven discriminator which provides an output voltage proportional to the tuning error (or carrier frequency drift). The discriminator output is applied as an error correcting signal to the reactance valve connected across the 2nd oscillator tuned circuit.

191. The output of the a.f.c. discriminator must depend on the frequency of its input only, and be independent of amplitude. To ensure this a pre-discriminator amplitude limiting stage V13 (Fig 34) is employed.

A.F.C. limiter, V13

192. The limiter operates with a low screen voltage and with a self-bias of value proportional to carrier amplitude. The input voltage is obtained from the anode of carrier amplifier V10 and is applied to the control grid via C69. R90 provides the grid bias.

193. As a check on carrier level, provision is made to monitor V13 grid current by switching the front panel meter across R91 and decoupling capacitor C70.

194. The constant amplitude limiter output is developed across T12 primary winding and coupled to the discriminator by the centre-tapped secondary.

A.F.C. crystal discriminator

195. The stabilization of a frequency to a high degree of accuracy, as required by the a.f.c. system of an s.s.b. receiver, demands a highly sensitive and stable discriminator.

196. Such circuits are either complicated, using frequency comparison and division systemsor comparatively simple using piezo-electric resonators evolved for the application but requiring complex alignment instruments. A piezo-electric resonator type has been designed for this receiver, which utilises a simple circuit and has the advantage of an adjustable cross-over frequency. (Fig 34).

197. Inductor L18 of transformer T12 is tuned by capacitor C73 to the nominal carrier frequency of 100kc/s. The bandwidth of this circuit is large compared with the useful frequency range of the discriminator so that the circuit may be assumed to be purely resistive over this range. L18 is centre tapped and the impedance of the two halves of the tuned circuit is low relative to the impedance connected to it and this tuned circuit is assumed, for explanation purposes, to be a centre

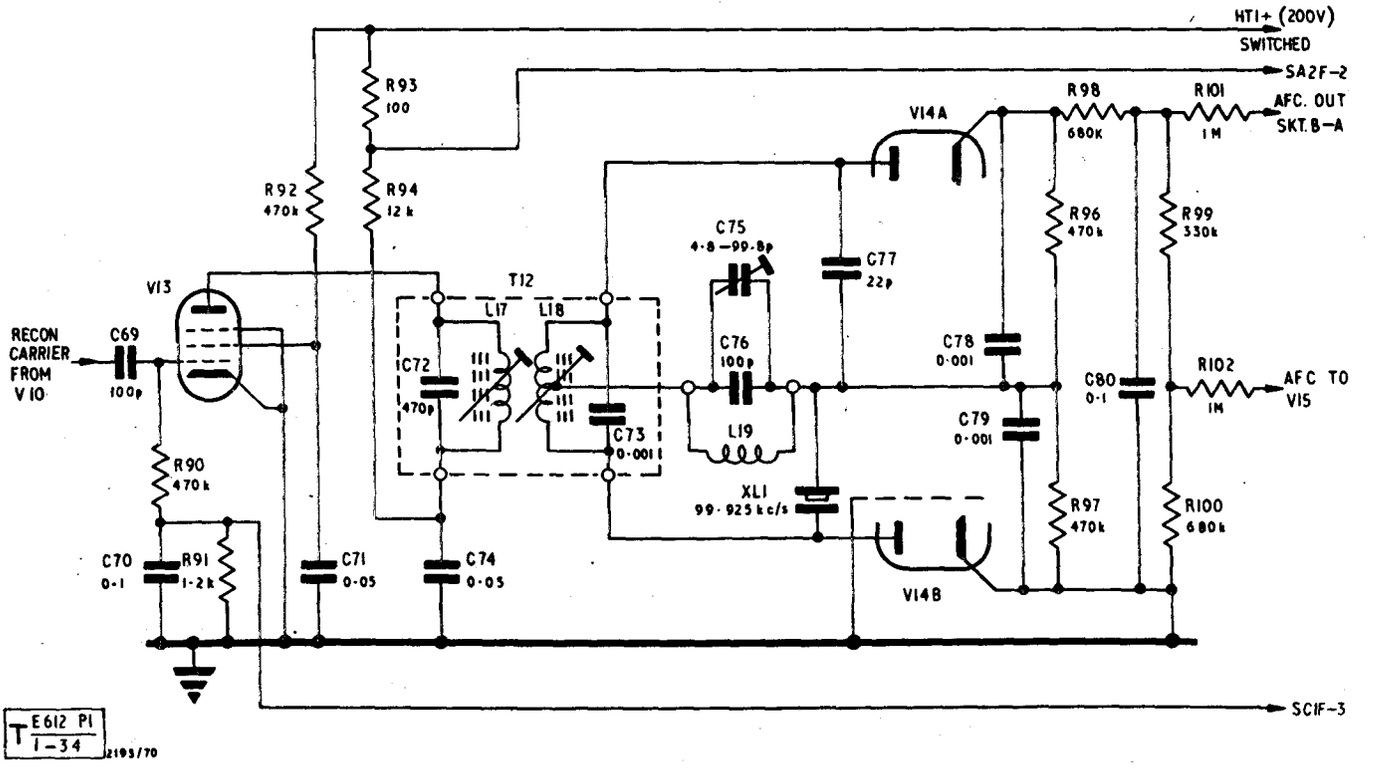

Fig 34 - A.F.C.limiter and discriminator, circuit diagram

tapped constant voltage source. L18 is loosely coupled to the primary of T12 (tuned circuit L17, C72 tuned to 100kc/s) in the anode circuit of the a.f.c. limiter V13. The coupling between L17 and L18 is less than critical since the looser the coupling the smaller the possibility of changes in the input circuit conditions affecting the discriminator performance. V14a and V14b are the sections of a double diode rectifier, R96 and R97 being their respective diode loads shunted by capacitors C78 and C79. XL1 is a piezo-electric resonator ground to operate at 99.925kc/s. C77 is included to balance the parallel capacitance of the crystal, Cp, and as far as current through C75 and C76 is concerned, the currents through C77 and Cp are equal and opposite, and therefore cancel.

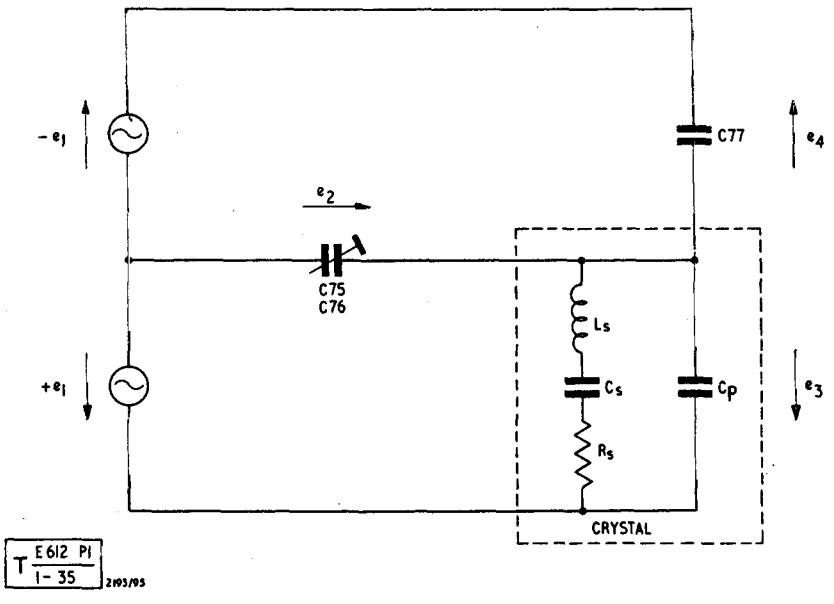

Fig 35 - A.F.C. discriminator, equivalent circuit

198. Fig 35 shows the equivalent circuit of the discriminator, with the crystal represented by its equivalent series components Ls, Cs and Rs. The parallel capacitance of the crystal is Cp. L19 is omitted from the figure as its reactance at 100kc/s is very much greater than the reactance of the capacitors across which it is connected, and it serves only as a d.c. return for the diode current. $+e_1$ and $-e_1$ are the input voltages supplied to the discriminator by L18. e_2 is the voltage developed across C75 and C76, and e_3 and e_4 are the voltages applied to the diodes.

199. Ls, Cs, Rs, C75 and C76 constitute a circuit which resonates at 100kc/s, 75c/s above the resonant frequency of the crystal. The frequency of maximum current

through C75 and C76 can be adjusted slightly by variation of the capacity of C75 so that this trimmer enables the cross-over frequency of the discriminator to be set to exactly 100kc/s.

200. Vector diagram Fig 36 shows the relationship of i_1, the current flowing through C75 and C76, to $+e_1$ and $-e_1$. At resonance, i_1 is in phase with $+e_1$. Below resonance, when the series circuit becomes capacitive, i_1 leads $+e_1$, and above resonance i_1 lags +e1.

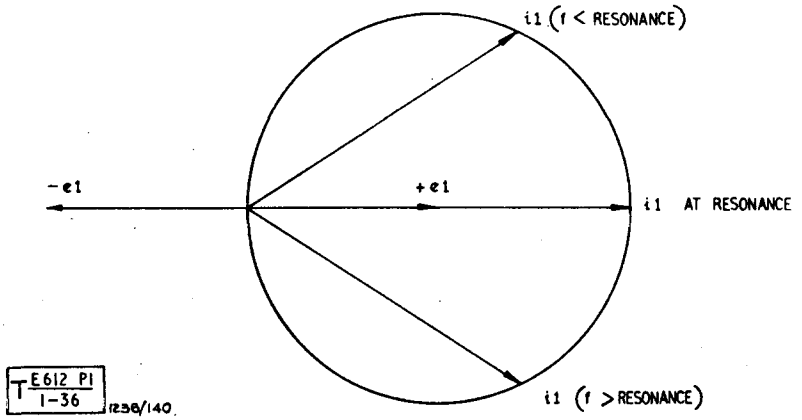

Fig 36 - A.F.C. discriminator, vector diagram, voltage and current relationships

201. Since e_2 always lags i_1 by 90° its magnitude and phase will vary in a similar manner to that of i_1 above, below and at resonance. Fig 37 shows vectorially the relationship between $+e_1$, $-e_1$ and e_2.

202. Vectorially, $+e_1 = e_2 + e_3$ and similarly $-e_1 = e_2 + e_4$. From this it can be seen that $e_3 = +e_1 - e_2$ and $e_4 = -e_1 - e_2$. At resonance, e_3 and e_4 are equal (Fig 38), the currents through the diodes are equal and the voltages developed across the diode loads are equal. Both cathodes go positive with respect to the junction of their loads by an equal amount so that V14a cathode is at earth potential (V14b cathode is earthed) and the a.f.c. line potential is zero with respect to earth.

203. Below resonance, the voltage e_4 applied to upper diode V14a is greater than e_3, and the voltage developed across R96 is greater than that across R97. V14a cathode is therefore more positive than V14b cathode with respect to the junction of their loads, and the output on the a.f.c. line is positive with respect to earth. Above resonance, e_3 is greater than e_4 and the voltage developed across R97 is greater than that across R96. V14b cathode is more positive with respect to the load junction than V14a cathode so that the a.f.c. output is negative with respect to earth.

204. Thus, the voltage applied to the a.f.c. line is dependent upon the direction of frequency variation from the nominal discriminator input of 100kc/s, and the magnitude of the voltage is proportional to the amount by which the input frequency deviates from 100kc/s.

205. R98 and C80 remove any residual voltage due to the 100kc/s carrier from the discriminator output, the whole of which is developed across potentiometer R99, R100. A portion of the output is fed to the s.s.b. tuning indicator stage.

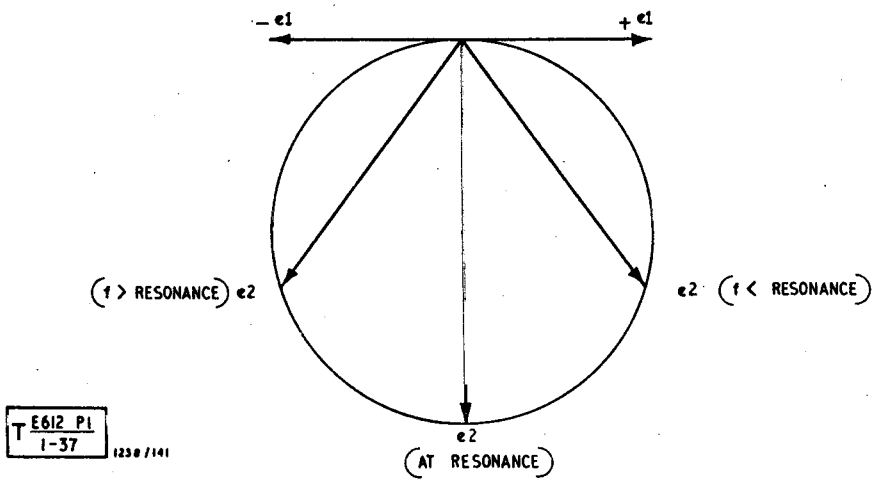

Fig 37 – A.F.C. discriminator, vector diagram, voltage across C75, C76 about resonance

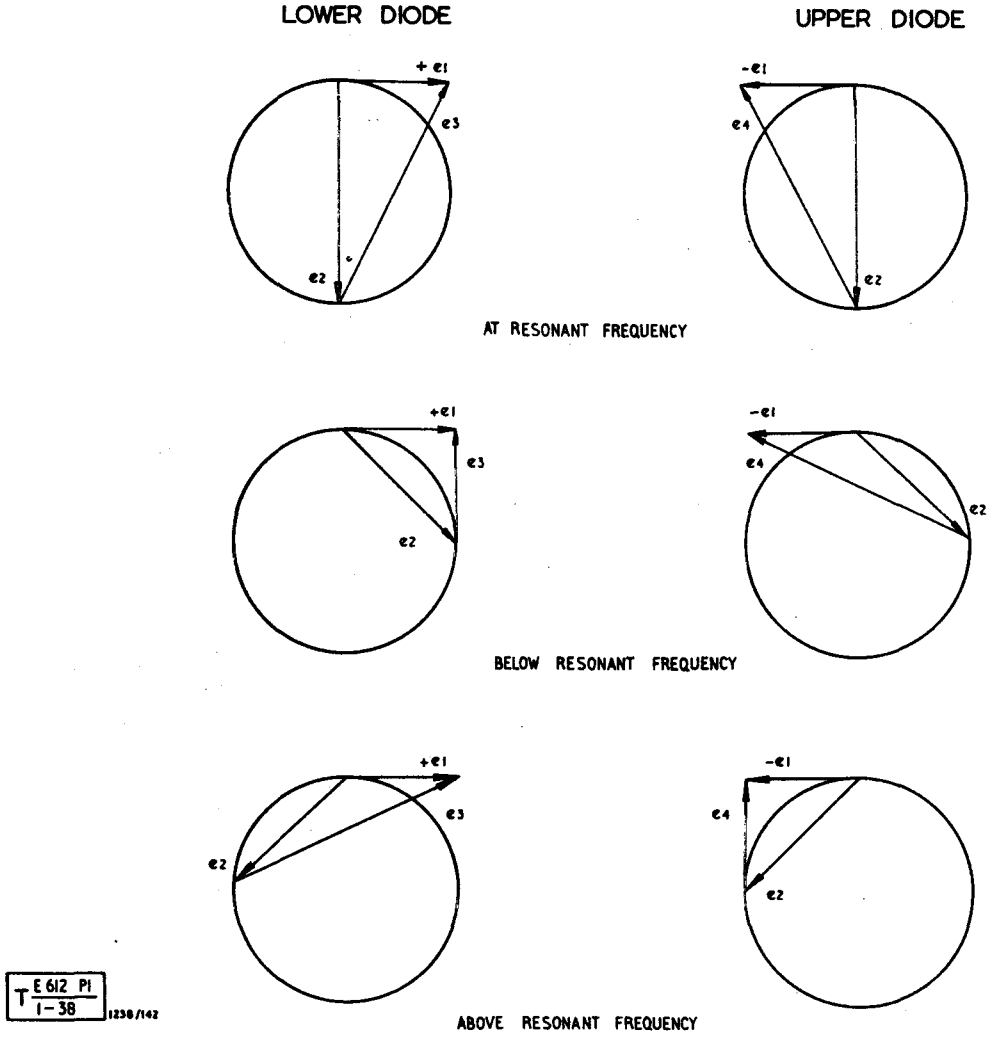

Fig 38 - A.F.C. discriminator, vector diagrams, output voltages about resonance

S.S.B. tuning indicator stage, V15

206. V15 is a double triode acting as a cathode coupled d.c. amplifier (Fig 39). A centre zero milliammeter, located on the front panel of the telegraph unit, is connected between its anodes. The cathode circuit is returned to -200V via R111. R170 ensures that the safe value of cathode/heater potential is not exceeded.

207. Under no signal conditions, the anode currents of the two halves of V15 can be equalized by adjustment of RV5. When the currents are equal, the meter reads centre zero.

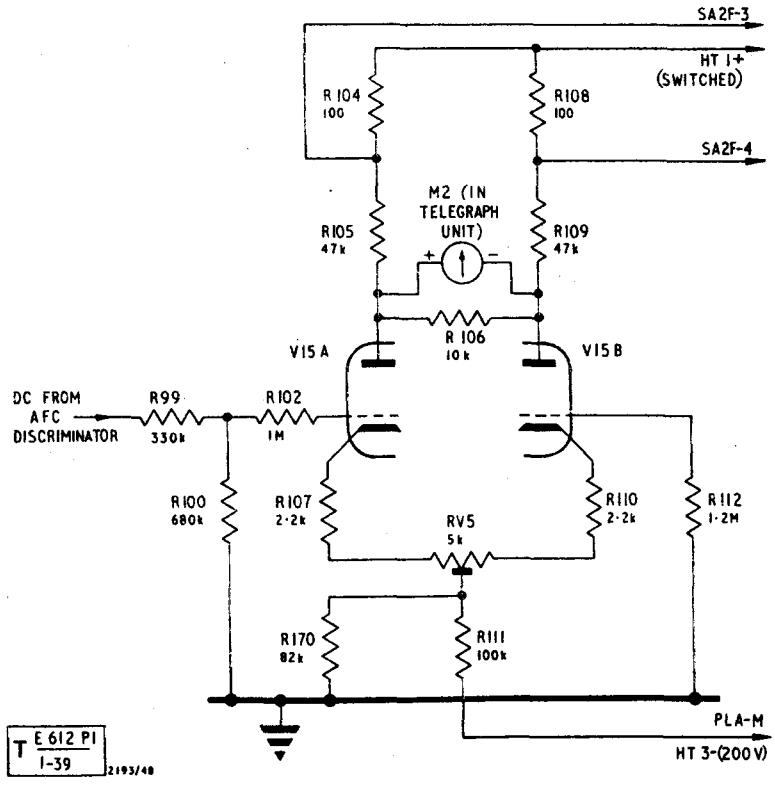

Fig 39 - S.S.B. tuning indicator stage, circuit diagram

208. When the 2nd i.f. input to the s.s.b. unit is precisely 100kc/s, the output from the a.f.c. discriminator, a portion of which is fed to V15a grid, is zero and consequently the meter is not deflected from centre zero, indicating that the receiver is on tune.

209. When the 2nd i.f. is lower than the nominal 100kc/s, the discriminator output voltage is positive with respect to earth, V15a anode current increases, the anode potential falls and a current flows through the meter and shunt R106. With a negative discriminator output the anode potential rises and the current and meter deflection are in the opposite direction. Thus the meter indicates the direction and amount by which the receiver is off-tune due to receiver mis-tune, oscillator drift or carrier drift.

A.G.C. system

General

210. A.G.C. bias can be applied to s.f. amplifier, V1 and to i.f. amplifiers, V3 and V4, in the s.f. and i.f.1 unit. For d.s.b., s.s.b. and i.s.b. reception the a.g.c. voltage is derived from the carrier amplifier in the s.s.b. unit. For f.s.k. reception and calibration purposes the control voltage is derived from the i.f.2

amplifier in the telegraph unit. For c.w. and suppressed carrier reception, the a.g.c. may be switched off and the gain of the controlled valves manually varied by RV4, HF GAIN control which applies a fixed bias to the a.g.c. line. Full details of the a.g.c. and gain control systems will be found at para 295. Fig 58 shows the composite a.g.c., manual gain control and desensitizing circuit.

A.G.C. rectifier, V16 (d.s.b., s.s.b. and i.s.b.)

211. Fig 40 shows the circuit of V16, a parallel connected double diode.

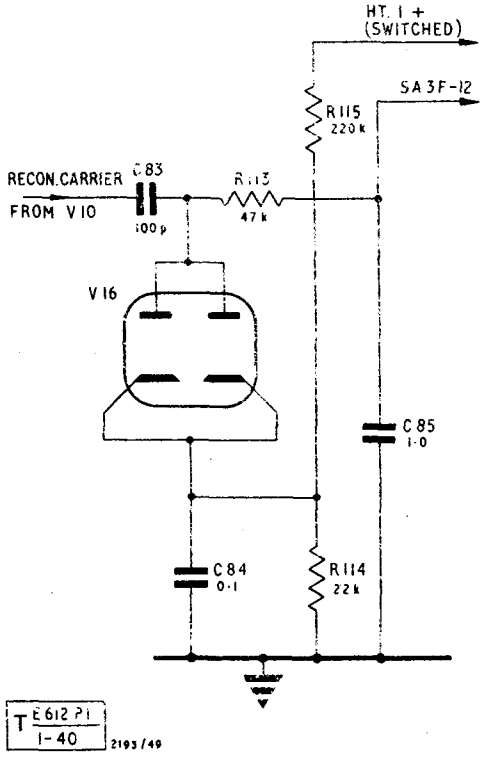

Fig 40 - S.S.B., a.g.c. rectifier circuit

212. Input to the rectifier is tapped off the carrier chain at V10 anode and coupled to V16 anodes by C83. The input level is proportional to the amplitude of the received carrier. A delay voltage of the order of +18V is applied to the rectifier cathode from potentiometer chain R114/R115 across HT1, 200V supply.

213. The d.c. output from V16 is connected to SA3F, system switch, telegraph unit, which selects the appropriate a.g.c. source for the reception system in use.

Monitoring facilities

214. Current monitoring resistors are included in all valve anode circuits, with the exception of V4, V14, V16, and V20, to allow anode currents to be monitored.

215. SA and SC switch front panel meter M1 across the current monitoring resistor of the selected valve. SC also connects M1 to the appropriate point for monitoring the carrier level at a.f.c. limiter V13, and the levels of sideband + carrier or sideband alone at demodulators V4 and V20. Meter switching (Fig 2509c) is effected by SC as follows:

(a) Positions 1 and 2: V1-V10 and V11-V22

SC1F connects the negative meter terminal to the appropriate wafer of SA. SC2F connects the positive meter terminal to the h.t.+ line.

(b) Position 3: CARR

SC1F and SC2F connect M1 across R91 decoupled by C70. The potential developed across R91 by V13 grid current is an indication of carrier level at the limiter grid.

(c) Position 4: U.S.B.+C

SC1F and SC2F connect M1 across R25 and R26, part of the u.s.b. demodulator load, thus monitoring upper sideband + carrier level at this point. SC1B switches shunt resistor R168 across the meter.

(d) Position 5: L.S.B.+C

SC1F and SC2F connect M1 across R154 and R155, part of the l.s.b. demodulator load, thus obtaining an indication of lower sideband + carrier level at this point. SC1B connects shunt resistor R168 across the meter.

(e) Position 6: U.S.B.

SC1F and SC2F connect M1 across R25 and R26, part of the u.s.b. demodulator load. In order that the sideband level only is measured, the screen supply to V6, reconditioned/local carrier amplifier, is removed by SC2B thus removing the carrier input to demodulator, V4.

(f) Position 7: L.S.B.

SC1F and SC2F connect M1 across R154 and R155, part of the l.s.b. demodulator load. In order that the sideband level only is measured, the screen supply to V22, reconditioned/local carrier amplifier, is removed by SC2B thus removing the carrier input to demodulator, V20.

Note: When SC is switched to U.S.B. or L.S.B. (position 6 or 7), severe distortion of the output signal occurs because of the removal of the carrier input to the demodulators.

Supplies

H.T.

216. All h.t. requirements are met by the HT1 (+200V) and HT3 (-200V) supplies. HT5 enters the unit merely for switching by SB.

L.T.

217. All valves are fed from the LT3 supply and, with the exception of V15, have 6.3V heaters. They are parallel connected in three chains, separately connected to PLA-E, PLA-F and PLA-G and earth. V15, 12.6V heater is centre tapped, the two halves being connected in parallel and connected across PLA-F and earth.

TELEGRAPH UNIT, TYPE 6637A
(Fig 2515-2520)

General

218. The special circuits required for single receiver and dual diversity telegraphy reception are contained in the telegraph unit. Also included are the sideband and monitor amplifiers, the telegraphy a.g.c. and a.f.c. circuits, the manual s.f. and audio gain control circuits, and part of the desensitizing circuit. System switching is carried out on this chassis by SA.

219. Transformers, filters, valves and other major components are mounted on the topside of the chassis, whilst the smaller items are secured to tagboards mounted on the underside. The chassis can be withdrawn from the cabinet and locked in an upright position for ease of maintenance.

220. Fig 41 is a general view of the unit. Immediately behind the front panel, from right to left, are mounted the f.s.k. tuning indicator stage, the output

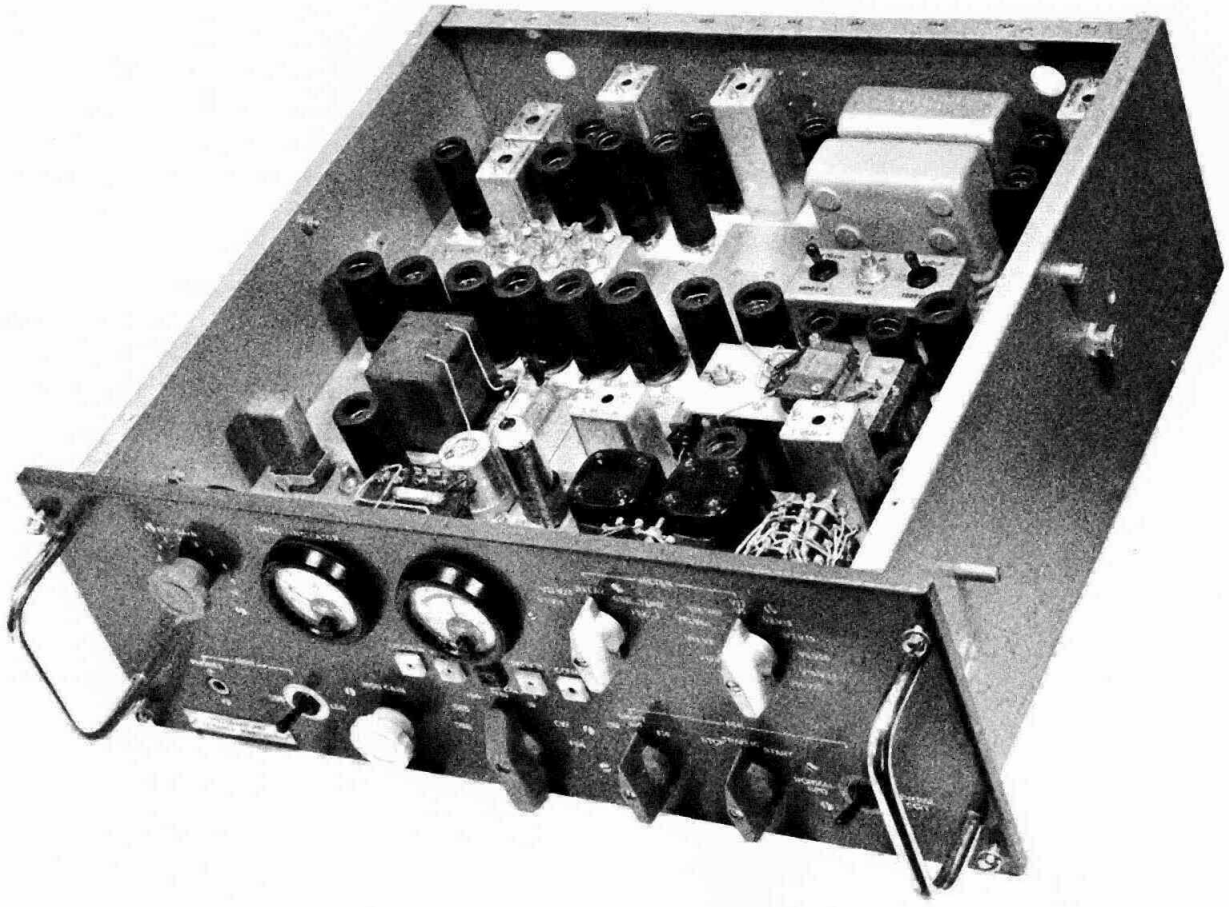

Fig 41 - Telegraph unit, general view

transformers and the line, monitor and a.f. amplifiers. The desensitizing relay is on the extreme left. From right to left along the centre are the 3kc/s amplifiers, the discriminator and the comparator and combining stages. Along the back from right to left are the telegraph filters, the second i.f. amplifiers, the third oscillator with its associated crystals, the third mixer and a.g.c. stages.

221. Fig 42 is a block diagram of the unit. Table 3 details the functions of the front panel and pre-set controls.

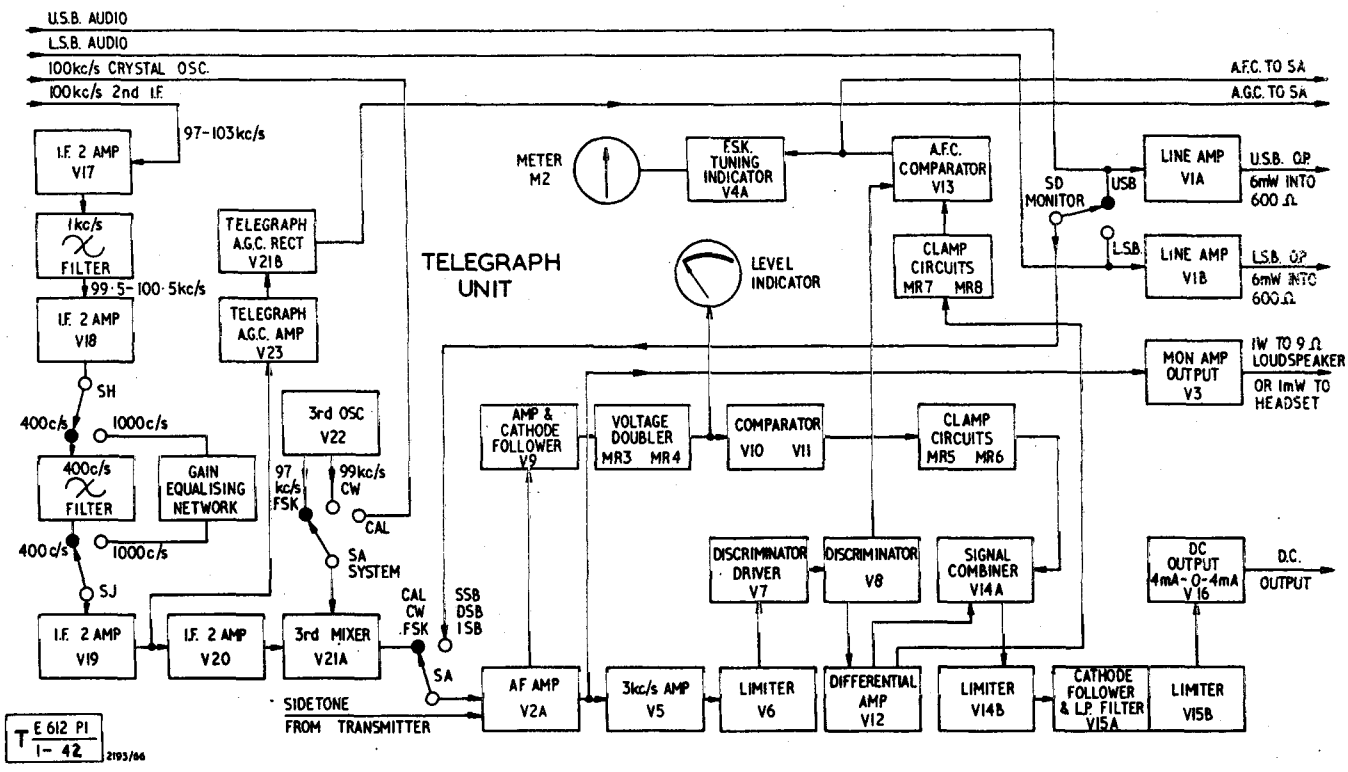

Fig 42 - Telegraph unit, block diagram

Filters

222. Two filters are used in the i.f.2 amplifier. The first in circuit operates between high impedance terminations as an intervalve coupling network. It is a two section half lattice type filter employing three crystal resonators and its nominal bandwidth is 1000c/s centred on 100kc/s. The filter is of miniaturised construction, hermetically sealed and temperature compensation is employed to maintain the performance over a wide range of temperature.

223. The second filter has a passband of 400c/s and is of the same type as that used in the carrier chain in the s.s.b. unit. Fig 2518 shows the filter response curves.

224. It is not possible to carry out any adjustments or repairs to the filters and no attempt must be made to open the containers. Any filter which has been proved faulty must be dealt with in accordance with EMER Tels A 801.

I.F. amplifier, V17-V20

225. Fig 43 shows the circuit of the i.f.2 amplifier which is common to c.w., f.s.k. and calibration working.

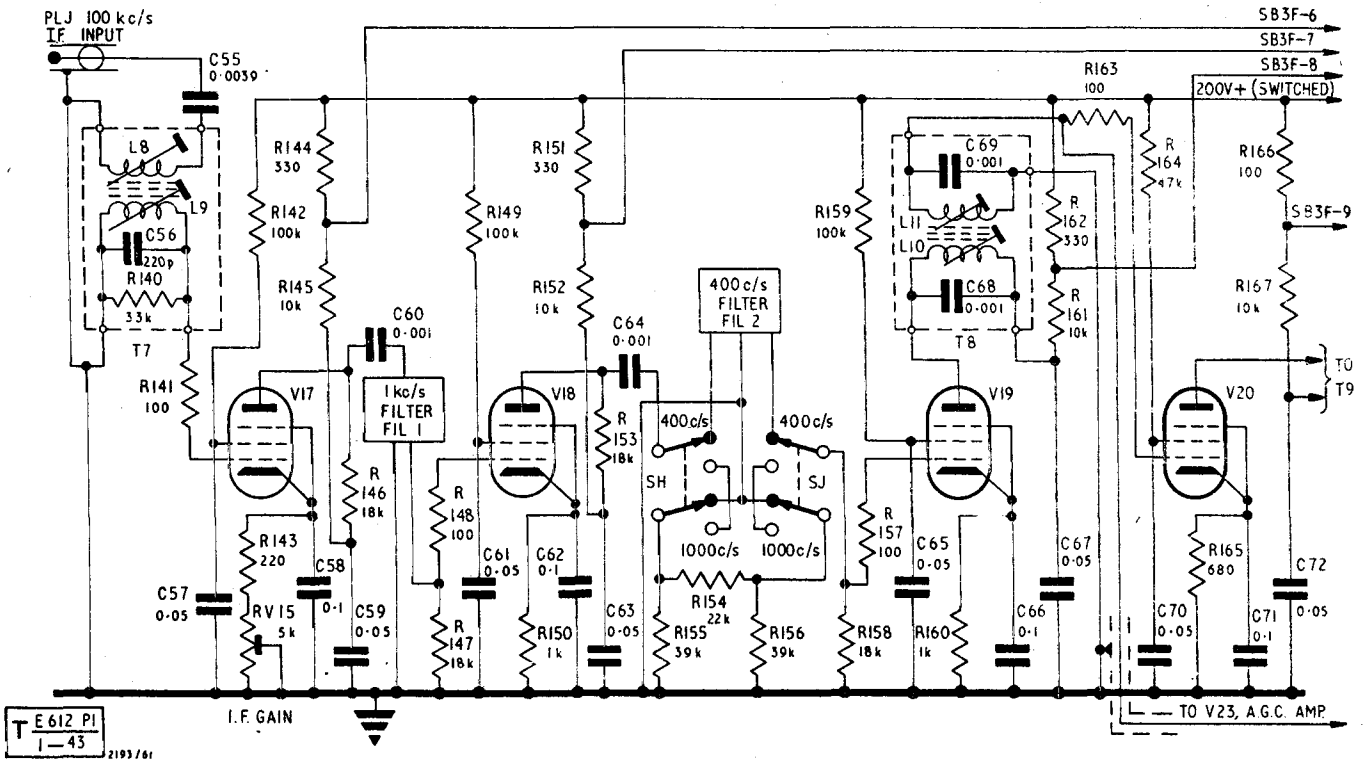

Fig 43 - I.F.2 c.w./f.s.k. amplifier, circuit diagram

226. The second i.f. signal is fed into the unit at PLJ and then applied to V17 grid via step-up transformer, T7. R143 and RV15 provide cathode bias for amplifier V17, RV15 being the chassis mounted pre-set i.f. gain control. V17 output is fed to FIL 1 via C60. V18 further amplifies the signal which is applied to SH by C64. With SH and SJ in the 400c/s position, as in Fig 43, the signal is coupled to V19 by FIL 2. With the switches in the 1000c/s position, the signal is attenuated by network R154, R155 and R156 before it is applied to V19. The attenuation of the network is the same as the insertion loss of the filter which must only be switched into circuit when receiving f.s.k. signals with a shift of 280c/s.

227. V19 and V20 further amplify the signal which is fed, via T9, to V21a for mixing with the third oscillator signal.

228. V23, a.g.c. amplifier (para 292) is fed from T8 secondary winding.

Third oscillator V22, and third mixer, V21a

General

229. The third oscillator (Fig 44) is crystal controlled. It comprises a two stage r.c. amplifier, V22a and V22b, with positive feed back from V22b anode to V22a grid via the crystal selected by system switch wafer SA7F.

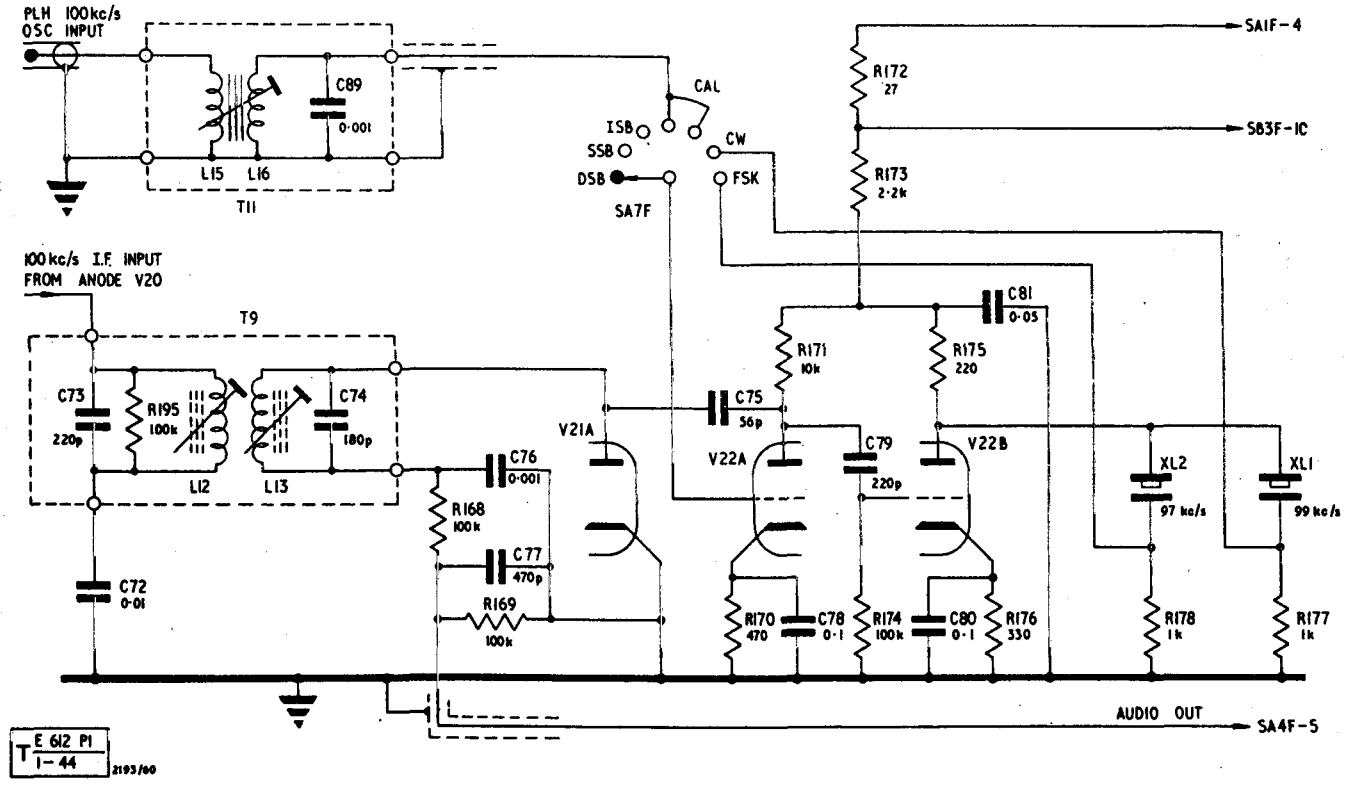

Fig 44 - Third oscillator and third mixer, circuit diagram

230. The third mixer stage uses a diode. The oscillator output is coupled to the diode anode by C75 and the second i.f. signal is fed to the same point by T9.

C.W. reception

231. When switched to CW, SA7F selects XL1 and the third oscillator runs at 99kc/s. The frequency of the signal from T9 is 100kc/s so that the difference frequency from the mixer is 1kc/s. This output is fed to the a.f. amplifier via SA4F.

F.S.K. reception

232. The oscillator operates at 97kc/s for f.s.k. reception. The frequency of the incoming signal from T9 is 100kc/s ± half the total shift frequency so that the frequency of the difference signal from V21a is centred on 3kc/s.

Calibrate

233. With SA at CAL 100 or CAL 10, the 100kc/s calibrator crystal oscillator signal is fed to V22a grid via T11 and SA7F. V22a amplifies the signal which is coupled by C75 to V21a mixer.

234. Also applied to the mixer is the second i.f. signal which is at 100kc/s when the receiver is correctly tuned. If the receiver is slightly de-tuned, the i.f. will differ from its nominal frequency and a mixer output will result, the frequency of which will increase with the amount of receiver off tune.

235. The mixer output is fed to the audio amplifier via SA.

Audio amplifier, V2a

General

236. V2a functions as an audio amplifier on all modes of reception and on c.w. transmissions when a sidetone signal is fed in from the transmitter. Fig 45 is a simplified circuit showing input selection and outputs.

237. Signals are applied to V2a grid via coupling capacitor C12 and a filter network,

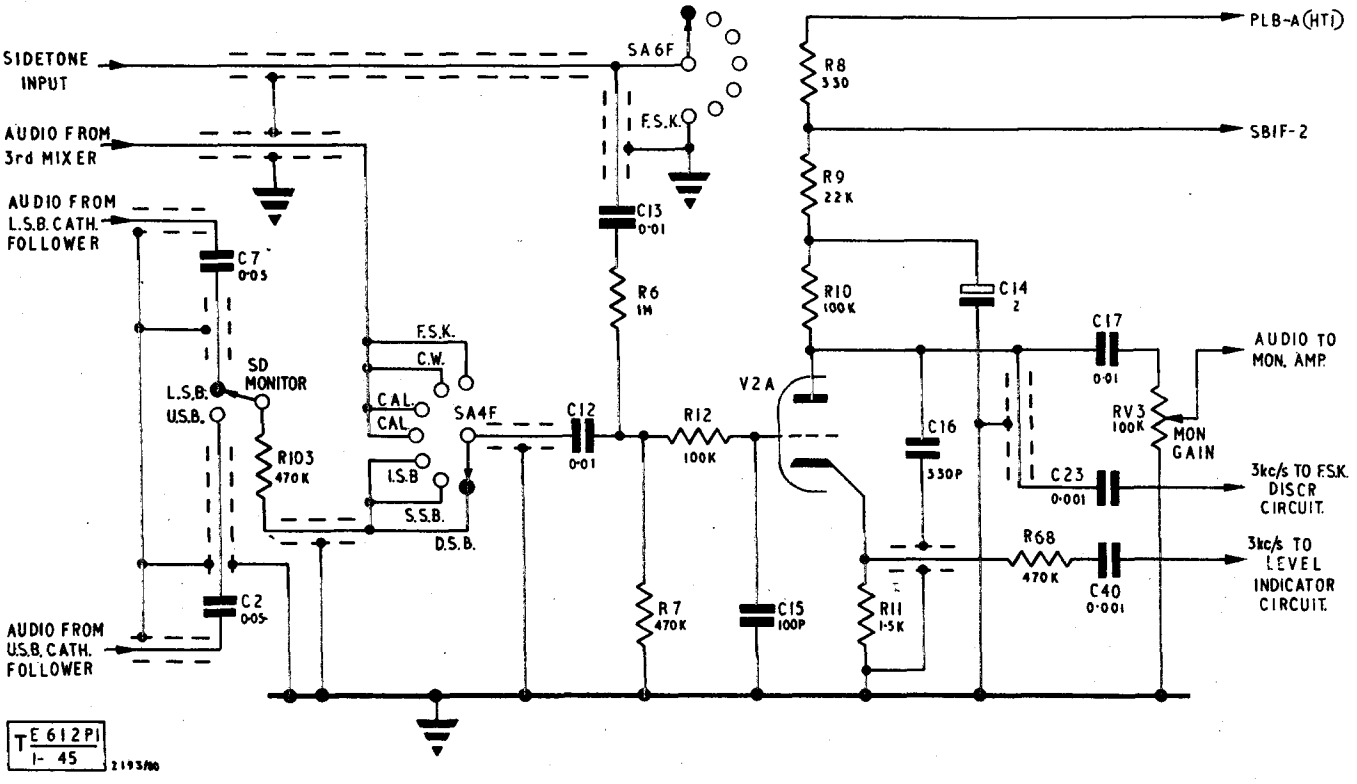

Fig 45 - A.F. Amplifier, circuit diagram

comprising R12 and C15, which is included to remove any residual third oscillator voltage from the amplifier input. In the anode circuit C16 provides further filtering. Use of an unbypassed cathode resistor provides negative feedback for the stage.

Inputs

C.W. reception

238. When SA is switched to CW, SA4F connects V2a input circuit to the third mixer output the frequency of which is 1kc/s for a correctly tuned signal.

F.S.K. reception

239. When SA is switched to F.S.K., SA4F connects V2a input circuit to the third mixer output the frequency of which is centred on 3kc/s for a correctly tuned signal.

Calibrate

240. When SA is switched to either CAL 100 or CAL 10 SA4F connects V2a input circuit to the third mixer output, the frequency of which depends upon the amount of receiver off-tune.

Telephony reception

241. When SA is switched to any of the three telephony positions, V2a input circuit is connected to SD the front panel MON switch. The position of SD determines which sideband audio signal is fed to V2a.

Sidetone

242. When operating on c.w., a keyed signal from the 1015c/s oscillator in the transmitter monitor unit is applied to V2a input circuit via C13 and R6. The signal enters the receiver at the TRANSMITTER plug on the distribution unit.

Output

243. The output signal is developed across RV3, front panel MON GAIN control, and applied to V3 monitor amplifier. The output is also fed to the discriminator and level indicating circuits which are only operative when SA is set to F.S.K.

Monitor amplifier, V3

244. The input level to V3 is controlled by RV3, MON GAIN (Fig 46). T5 output transformer drives the monitor loudspeaker which is connected to the low impedance secondary, winding via SKTF-G, SKTF-H (earth), the distribution unit and the control indicator. The speaker impedance is 9Ω.

245. JKA is mounted on the telegraph unit front panel for headset use. When the jack plug is inserted in JKA, the feed out to the speaker is disconnected and dummy

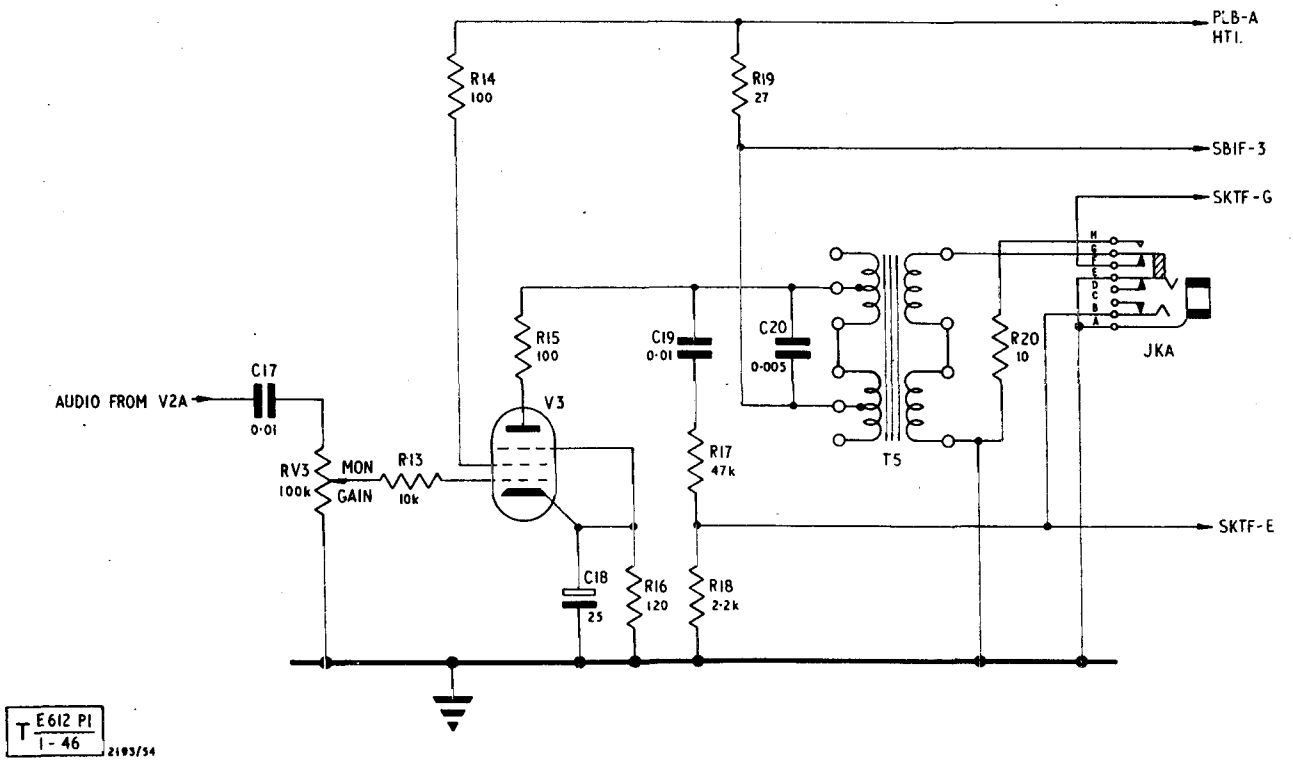

Fig 46 - Monitor amplifier, circuit diagram

load R20 is shunted across T5 secondary winding. The portion of the output developed across R18 in V3 anode circuit is fed to JKA and to the distribution unit via SKTF-E and SKTF-F (earth).

3kc/s amplifier, V5 and limiter, V6

246. The 3kc/s f.s.k. output from V2a is applied to amplifier V5 via C23, (Fig 47). The unbypassed cathode resistor R40 provides negative feedback to assist the stage to handle large input signals. However, with very large input signals grid current limiting will take place during positive half cycles of the input signal the limiting level being determined by the value of V5 cathode bias. To obtain approximately symmetrical limiting, diode MR2 is included in V5 grid circuit to limit the negative excursions of the signal, the limiting level being set by the voltage at which MR2 conducts.

247. V5 output is coupled to V6a grid by C25. V6a and V6b act as a limiter and are basically a cathode follower coupled to an earthed grid amplifier by the common unbypassed cathode resistor, R49. The advantage of this type of limiter lies in the fact that there are no capacitors to be charged in the squaring circuit so that the circuit time constant is reduced to a minimum.

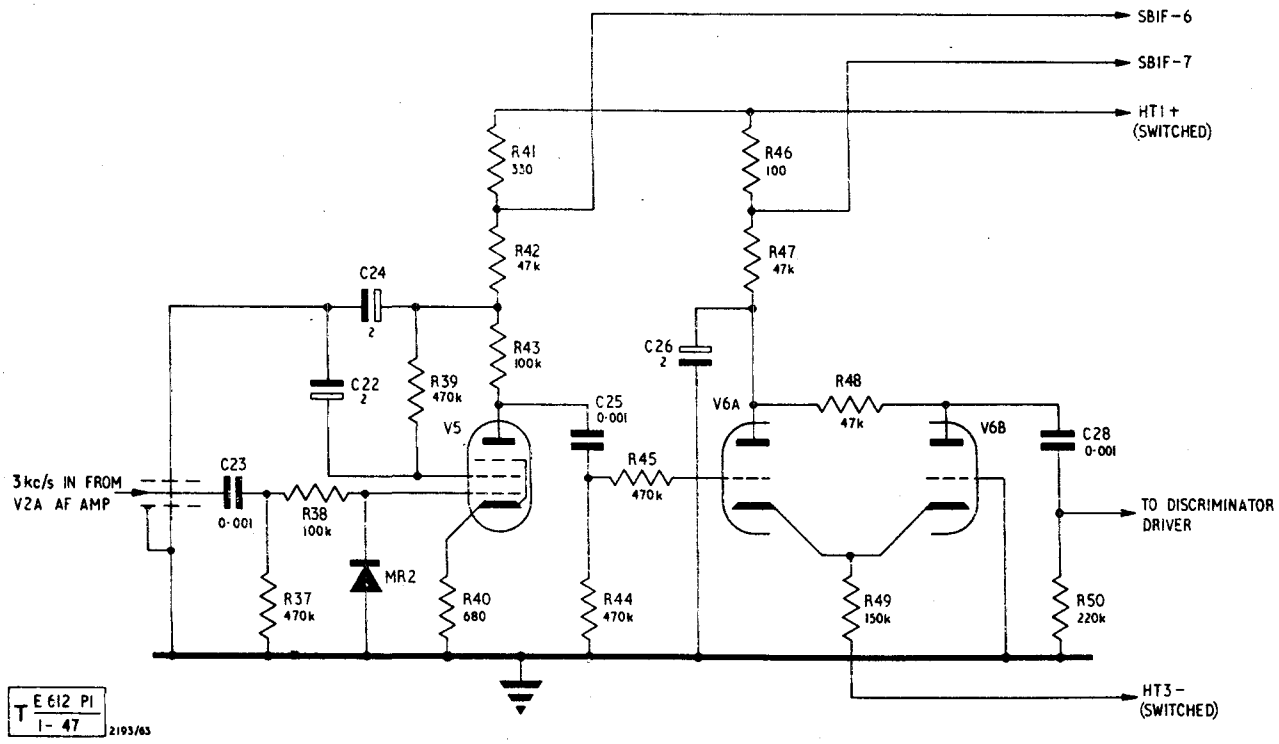

Fig 47 - 3kc/s amp and limiter, circuit diagram

248. The combined valve currents flowing through R49 produce a static bias which locates the working points of the triodes in approximately the centre of their mutual characteristic curve under no signal conditions. Large positive peaks to V6a grid cause the cathode potential of the triodes to rise and consequently V6b anode current cuts off. V6a grid current is limited by R45. Large negative peaks at V6a grid cause V6a to cut off and V6b conducts heavily resulting in a drop in the potential at the anode. The limiter output is coupled to the grid of the discriminator driver via high pass and low pass filter networks.

Discriminator Driver, V7 and Discriminator, V8

249. C28 and R50 (Fig 48) form a high pass filter with a cut-off frequency just above 3kc/s. C27 and R51 comprise a low pass filter with cut-off frequency just below 3kc/s. Any asymmetry in V6b output tends to be corrected by the filters which round off the edges of the signal and modify the waveform to a suitable shape for application to the discriminator.

250. V7 anode circuit and V8a and V8b form a Foster-Seeley discriminator (EMER Tels A 013) which is tuned for a cross-over frequency of 3kc/s by C34. To ensure that the 3kc/s tuning point lies within the range of C34, C36 and C37 can be linked in or out of circuit as required.

251. The diode outputs, which are developed across R57 and R58, are connected in

opposition and the resultant output is proportional to the input frequency relative to cross-over frequency. At cross-over frequency, the diode outputs are equal and opposite and the resultant output is zero. At frequencies greater than 3kc/s, the output from V8a will predominate; at frequencies below cross-over, V8b output is the greater.

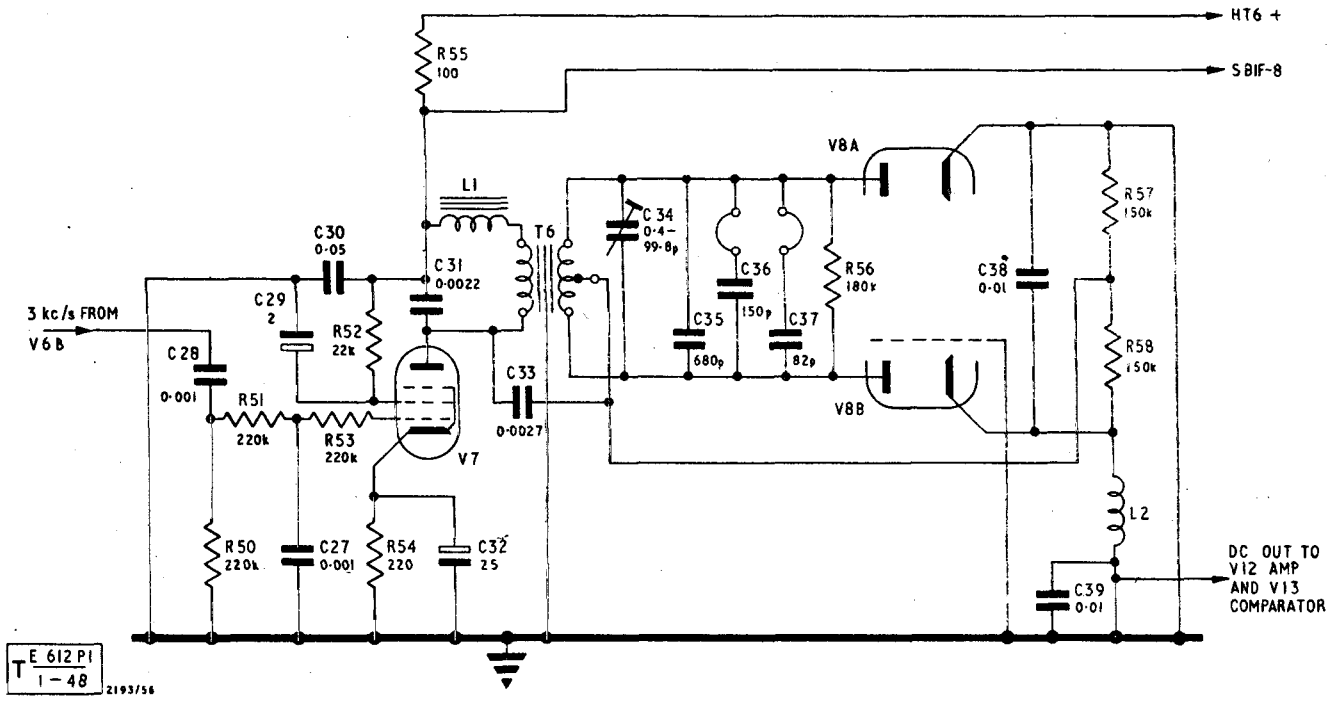

Fig 48 - Discriminator driver and discriminator, circuit diagram

252. The discriminator output follows the original modulating signal and since V8a cathode is at earth potential, the mark and space potentials are equally positive and negative with respect to earth. Any one of three frequency shifts may be employed when working f.s.k., 280c/s, 400c/s or 850c/s, and the amplitude of the discriminator output increases with the shift frequency.

253. L2 and C39 form a low pass filter which is included to remove any 3kc/s component remaining in the signal which is applied to V12a for signal purposes and to V13b for a.f.c. purposes.

V12, Differential amplifier

254. V12 (Fig 49) is a double triode acting as a cathode coupled d.c. amplifier designed to handle large input signals and to provide a square wave output of approximately ±30V. The f.s.k. discriminator output is fed to V12a grid and outputs from V12b anode are taken to V13a for a.f.c. purposes and to V14a in the signal path.

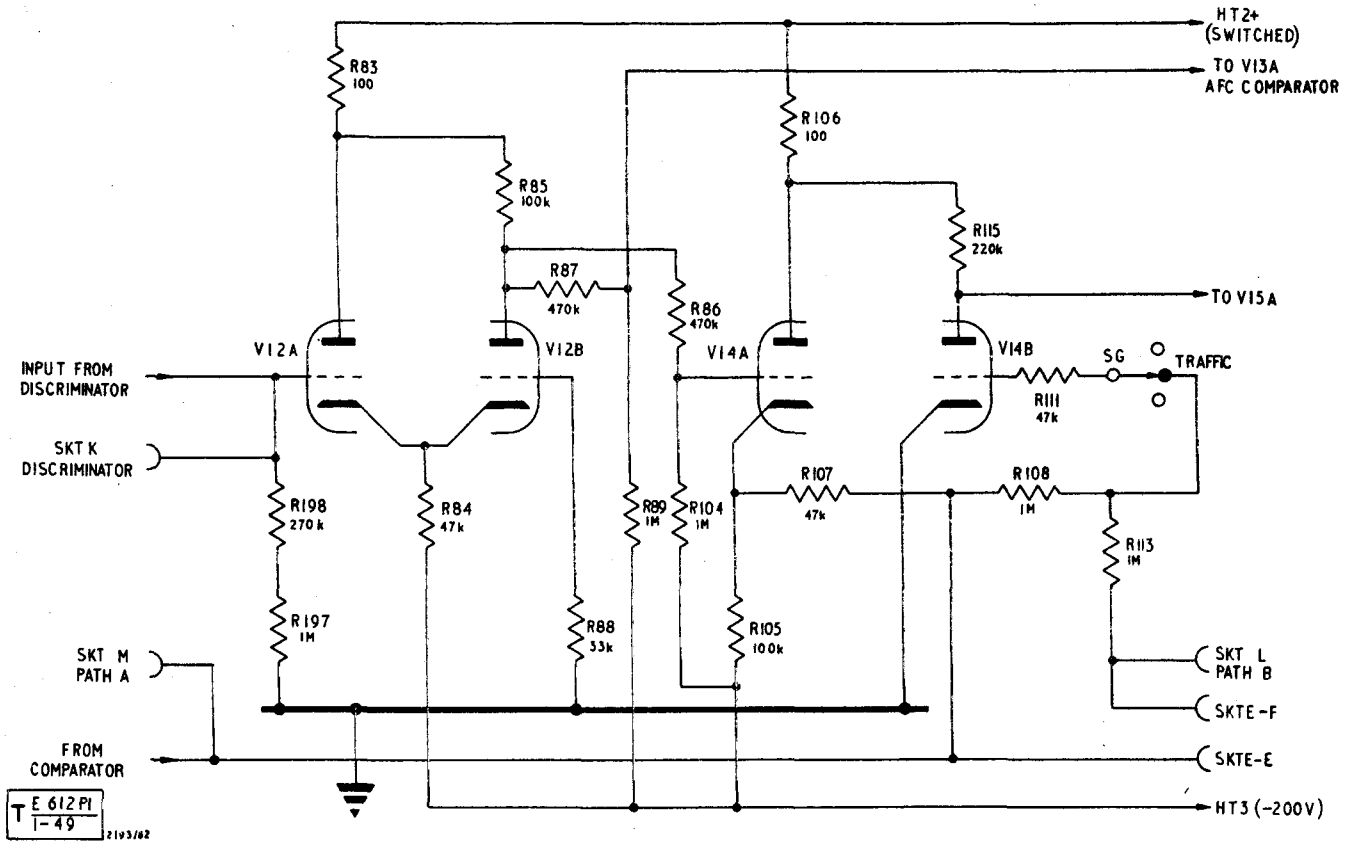

Fig 49 - Differential amplifier and signal combiner, circuit diagram

V14, Signal combiner

255. V14a is a cathode follower which forms part of the signal combining circuit which is only fully used when the receiver is working in dual diversity. Under these conditions the telegraph signals from the signal combiner of the second receiver are fed into the cathode of V14a. At the same time, the telegraph signal output from V12b is applied to V14a grid.

256. Under single receiver working conditions, V12b output is applied to V14a grid, and the square wave output at the cathode of V14a is clamped at levels determined by the comparator stages, V10, V11 and clamp circuits, MR5, MR6 (para 290). These levels are ±30V, and since the output of V12b is a square wave of magnitude ±30V, the comparator circuits have little effect on single receiver performance.

257. The output signal from V14a is applied to V14b via f.s.k. test switch SG at TRAFFIC. V14b is a limiter employing grid current and anode current cut-off limiting. The output is directly coupled to the grid of limiter V15a by signal bias control RV14.

258. For test purposes SG can select and connect bias voltage simulating mark and space conditions to V14b grid in place of the received telegraph signal (para 265).

259. SKTK , SKTL, and SKTM are front panel mounted sockets for waveform monitoring. SKTE-E and SKTE-F are connected to the distribution unit. They are used only when the receiver is working in dual diversity.

Limiter V15 and d.c. output stage, V16

260. V15a is a cathode follower with its cathode load returned to -200V (Fig 50). To restrict the heater/cathode potential to a safe level, R118 is strapped between cathode and earth.

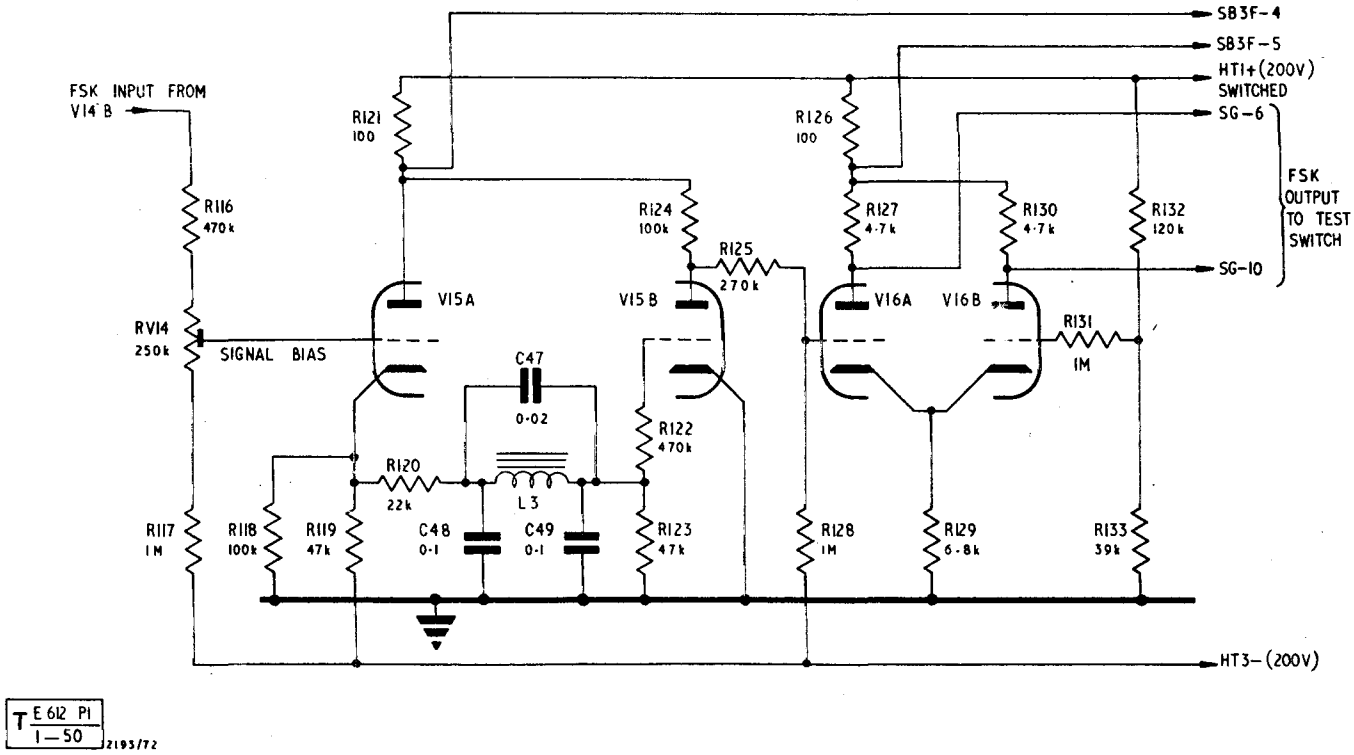

Fig 50 - Limiter and d.c. output stage, circuit diagram

261. Before the signal is applied to V15b, it is fed through a low pass filter comprising L3, C47, C48 and C49. This filter restricts the bandwidth of the signal to the optimum value for the maximum keying speed used, and also provides protection against impulse interference. The signal waveform is modified by the filter which gives it a sloping wavefront enabling control of the signal bias to be effected by adjustment of the slicing level of V15b, by RV14.

262. Signal bias control RV14 forms part of a potentiometer chain connected across the HT2 and HT3 supplies, and adjustment of this control varies the standing

potential of V15a grid and consequently the standing cathode potential. V15b grid is directly coupled to V15a cathode by R120, L3 and R122 so that RV14, although in V15a grid circuit effectively controls V15b grid bias.

263. V16 is a cathode coupled double triode d.c. amplifier. V15b output is directly coupled to V16a grid. In the STOP (mark) condition, V16a is cut off and V16b is fully conducting. Application of a positive going START (space) signal to V16a grid drives the valve to its fully conducting state, while V16b is simultaneously cut off. The 4-0-4mA output is fed via SG (F.S.K. test) and SE (F.S.K. keying) to the distribution unit and thence to a polarized relay external to the receiver.

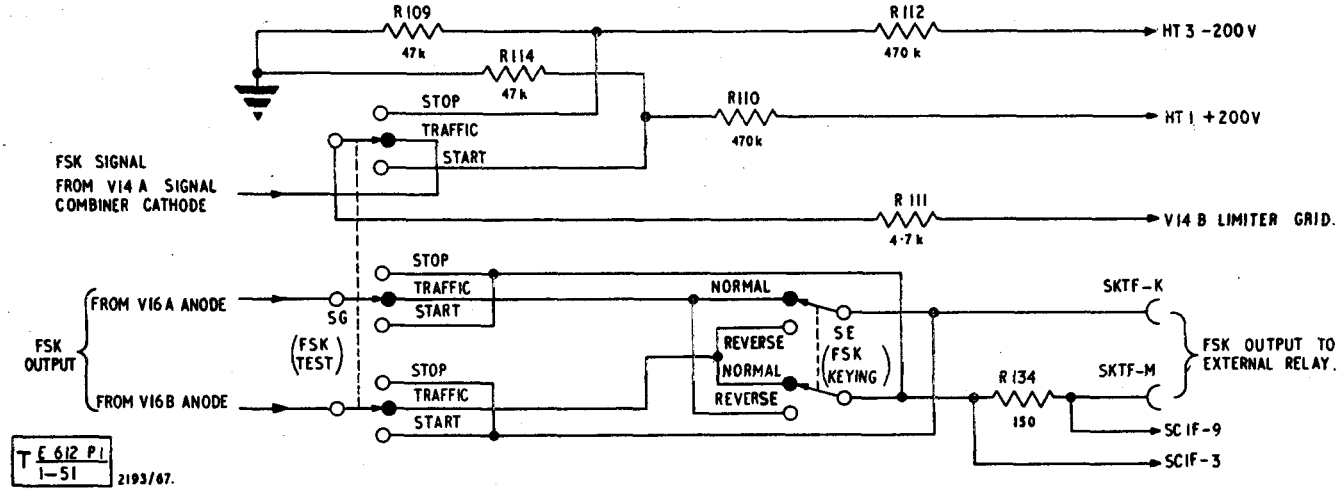

Fig 51 - F.S.K. keying switch and test switch, simplified circuit diagram

F.S.K. switching

SG (F.S.K. test) and SE (F.S.K. keying)

264. Fig 51 shows a simplified circuit of SG and SE.

SG

265. When SG is switched to STOP, one pole connects a negative bias derived from R112 and R109 connected between earth and -200V, to V14b grid. In the START position a positive bias derived from R110 and R114 is connected to V14b grid. These two conditions selected by SG simulate STOP and START (mark and space) conditions and are used for functional tests of the output stage.

266. The two other poles of SG connect the output from the d.c. output stage to the distribution unit via SKTF-K and SKTF-M on either the START or STOP position. At TRAFFIC the f.s.k. output is connected to SE (F.S.K. keying).

SE

267. The function of SE is to provide an output signal which will conform to B.P.O. or C.C.I.T. standards in respect of mark/space polarity.

268. R134, in series with V16a output or V16b output depending upon the position of SE, is used when monitoring the telegraph relay current. When in the RELAY position SC connects M2 across R134.

Telegraph a.f.c. system

General

269. The reactance valve is controlled by a d.c. biasing potential proportional to the tuning error, which would normally be derived from the output of a carrier driven discriminator as in the case of telephony a.f.c. However, discriminator V8 is tuned to a centre frequency of 3kc/s and the actual input signals are at frequencies differing above and below the centre frequency by half the total shift, for a correctly tuned signal. The discriminator output therefore consists of positive and negative potentials corresponding to the mark and space signals, the amplitude of which increase with frequency shift, and which also vary with the degree and direction of tuning error. An output in this form is not suitable for direct application to the reactance valve and intermediate circuits are required to produce an output which can be fed as a smooth bias to the valve.

270. To derive the required bias voltage, two signals are fed into V13, a.f.c. comparator. The discriminator output is fed to one portion of the comparator whilst a signal clamped at the levels which would be produced by a correctly tuned signal is applied as a reference signal to the second portion of V13. The comparator is designed to produce a d.c. output proportional t the difference between the reference signal level and the discriminator output level and this output is applied as an error correcting voltage to the reactance valve. The magnitude and sense of this voltage is shown by the front panel mounted centre zero meter, M2.

271. Use of the a.f.c. system reduces frequency drifts of up to 3kc/s to less than 10% of the total shift.

Clamp circuits, MR7 and MR8

272. V12b provides square wave outputs at levels of + and -30V. These are applied via R87 to clamping diodes MR7 and MR8 and associated circuits (Fig 52). MR7, which provides the positive clamping level, is biased by one of three potentiometers connected between HT6 (+150V) and earth. F.S.K. SHIFT switch SF selects the potentiometer.

273. MR8, biased by one of three potentiometers connected between HT7(-150V) and earth, provides the negative clamping level. SF again selects the appropriate potentiometer.

274. Clamping levels are adjusted by the pre-set variable resistors in each potentiometer chain to equal the levels obtained by a correctly tuned signal at the output of the discriminator.

275. The output signal from the clamp circuit is applied to V13a grid as a reference signal.

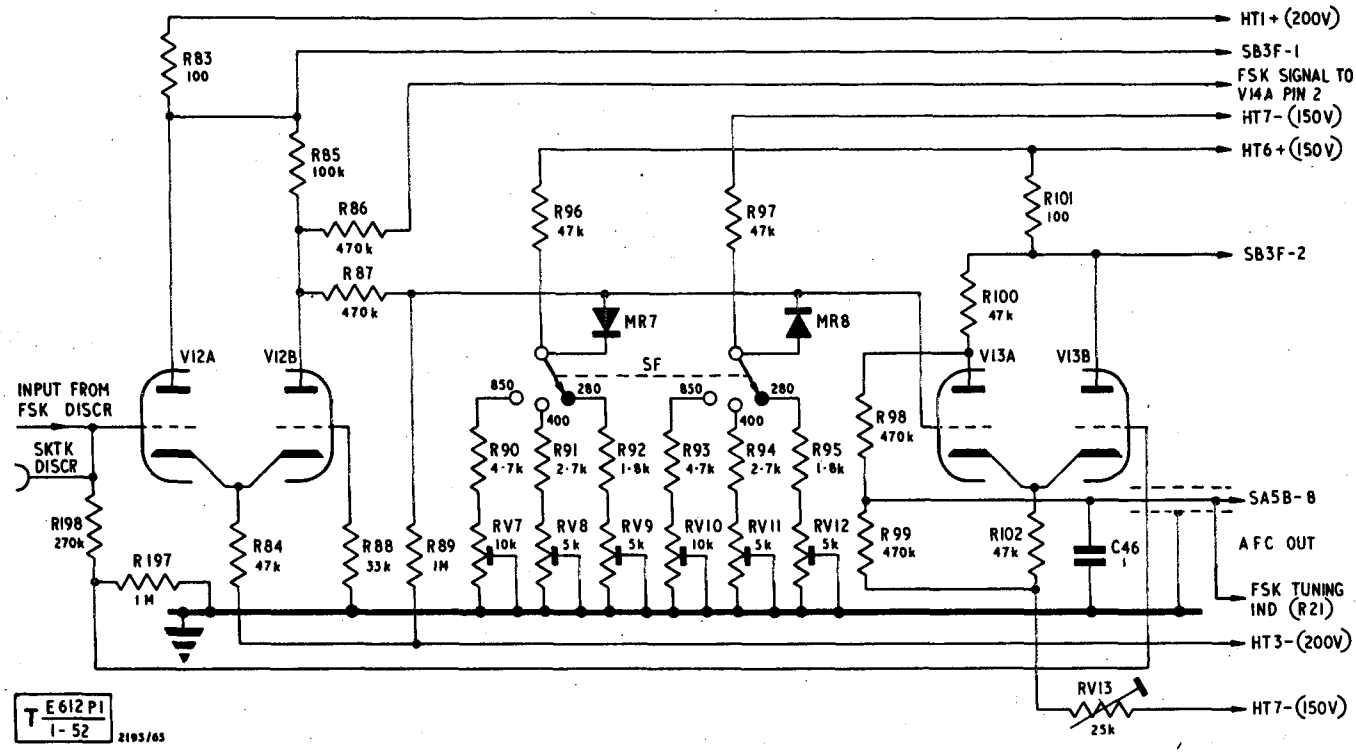

Fig 52 - Clamp circuit and a.f.c. comparator, circuit diagram

A.F.C. Comparator, V13

276. The a.f.c. comparator comprises a cathode coupled double triode, V13a and V13b. Two inputs are applied to the valve, and these act in opposition to each other.

277. The reference signal is applied to V13a grid and a portion of the output from the discriminator is fed to V13b grid.

278. For a correctly tuned signal, the output level of the signal from the discriminator will be equal to the reference signal level, and there will be zero output from the comparator.

279. If one of the receiver oscillators or the transmitter frequency drifts slightly the discriminator output will alter; for an upward frequency drift the positive output will increase and the negative output will go less negative by the same amount. The input voltage applied to V13b now differs from the reference voltage applied to V13a, and the resultant output is tapped off the potentiometer chain connected between V13a anode and HT7, and taken to SA for selection and to V4a f.s.k. tuning indicator stage. C46, 1μF, gives the output circuit a long time constant.

280. RV13 enables the output level of V13a to be set to zero under no signal conditions.

281. Fig 53 is a simplified circuit of the receiver a.f.c. system showing selection and distribution.

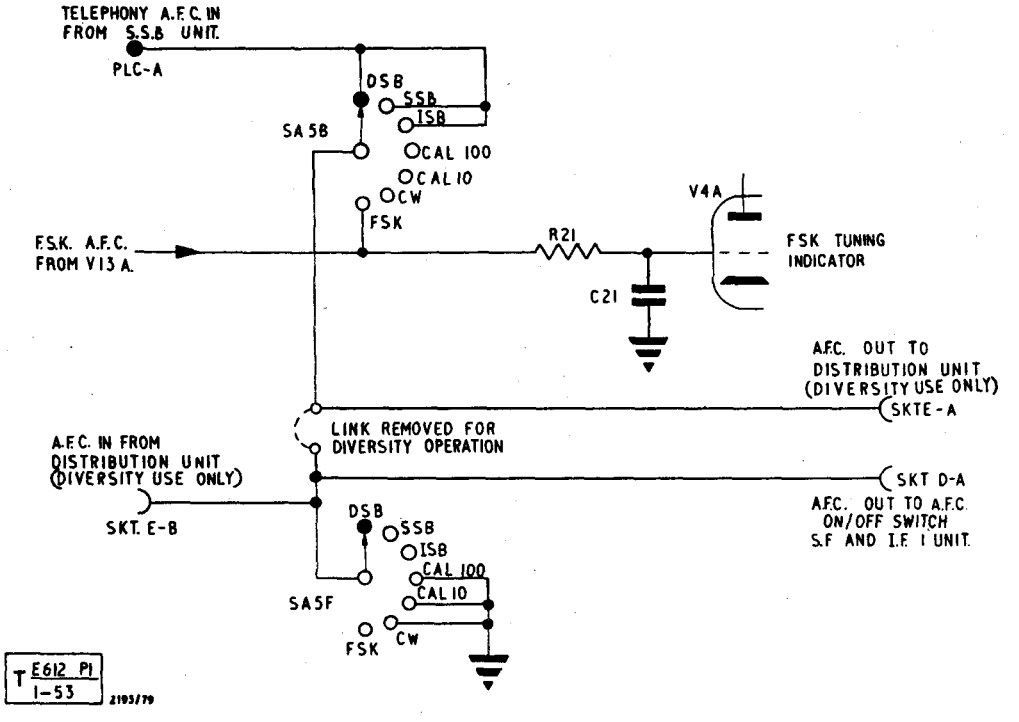

Fig 53 - A.F.C. selection and distribution, simplified circuit diagram

F.S.K. tuning indicator stage, V4

282. The f.s.k. tuning indicator stage uses a cathode coupled double triode d.c. amplifier, with a centre zero milliammeter connected across its cathodes (Fig 54).

283. The a.f.c. voltage from V13 which is applied to the reactance valve, is also applied to V4a grid via a long time constant circuit R21, C21, included to stabilize the movement of the meter pointer. The meter is connected to the cathodes by SC1F-5 and SC1F-11 in the TUNE F.S.K. position of the switch.

284. Common cathode resistor R25 is returned to HT3 (-200V) and one side of the heater is returned to earth. To prevent the cathode/heater potential exceeding a safe value, R22 is connected between the junction of RV5/R25 and earth.

285. Meter zeroing is effected by RV5 which is adjusted to equalize the current drawn by each section of the valve under no signal conditions. This current balance will be upset when there is an output from V13, and the meter will be

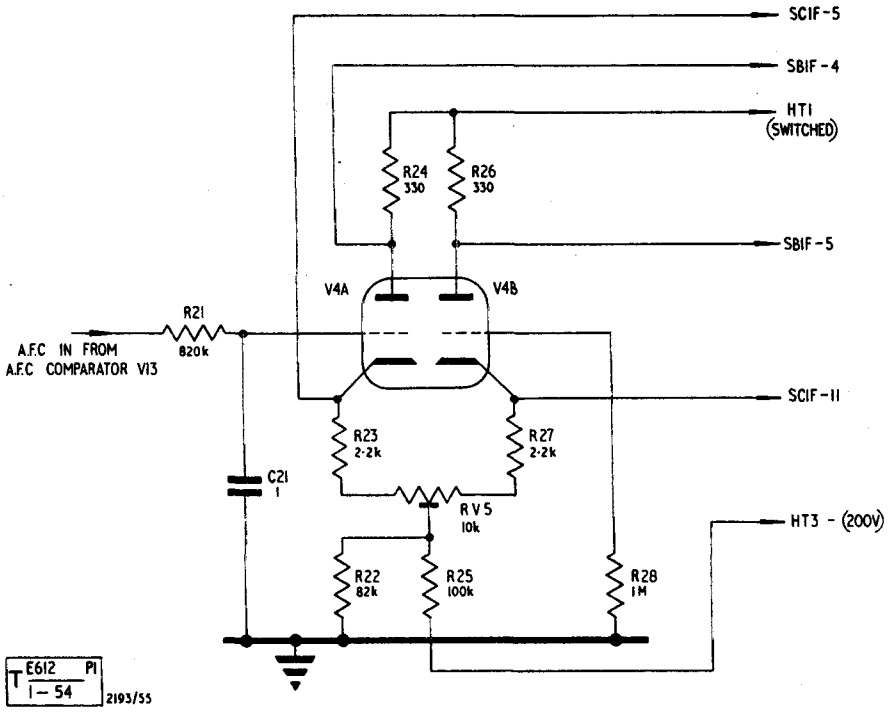

Fig 54 - F.S.K. tuning indicator stage, circuit diagram

deflected from its centre zero position in accordance with the polarity and magnitude of the input voltage. A negative input causes a deflection to the right.

286. The polarity of the a.f.c. voltage depends upon the direction of receiver off-tune and its magnitude is proportional to the amount by which the receiver is off-tune. The meter therefore indicates residual tuning error.

Level indicating circuit

287. An f.s.k. output centred on 3kc/s is obtained from the cathode of audio amplifier V2a and coupled to V9a amplifier grid by C40 (Fig 55). The output of V9a is applied via cathode follower V9b and C43 to a rectifier circuit comprising MR3, MR4 and associated components.

288. The output of the rectifier circuit is negative d.c. of magnitude proportional to the level of the 3kc/s input which is proportional to the level of the received signal. Meter M1 is in series with MR4 load R67, thus providing a direct indication of signal level. Meter scale calibration is in dB.

289. The d.c. output is also taken to V10 comparator and to the distribution unit via SKTE-C for use when working dual diversity.

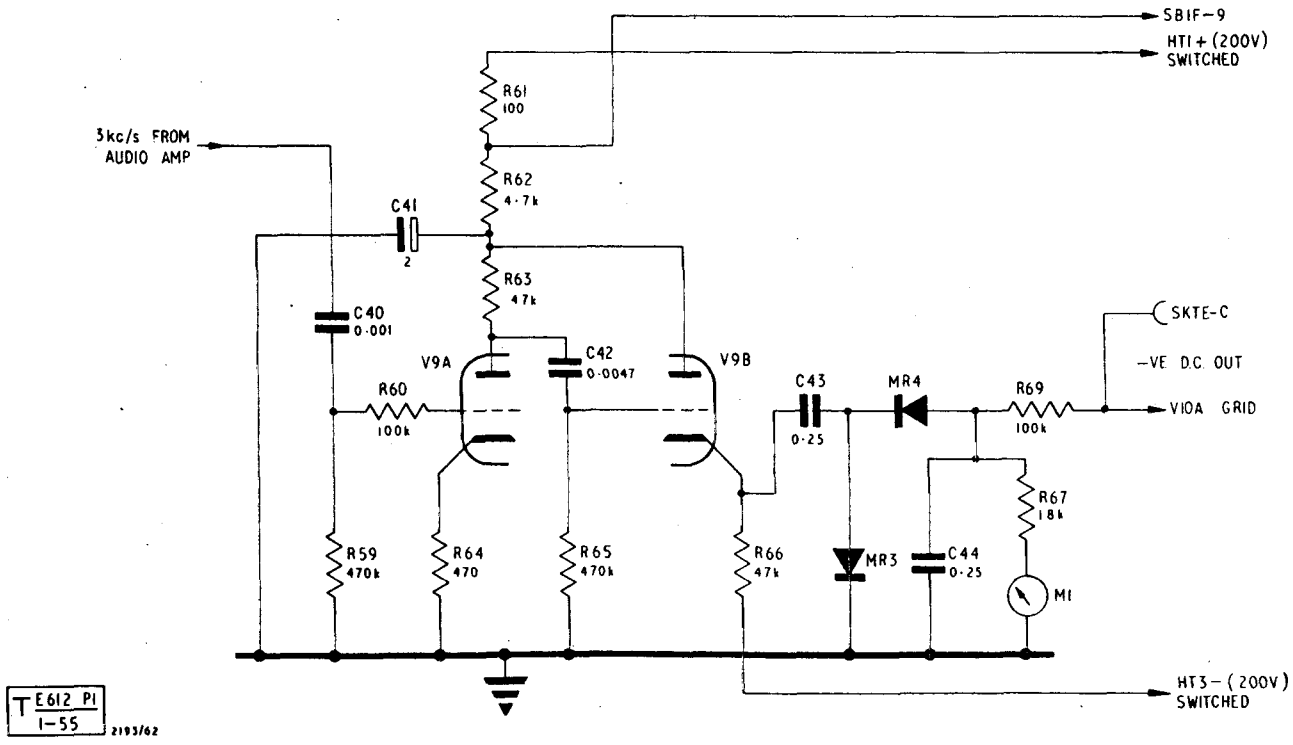

Fig 55 - Level indicating stage, circuit diagram

Comparator V10, V11

290. The comparator stages (Fig 56) are only fully utilized when working dual diversity. Under these conditions double triode V10 acts as a form of differential amplifier with d.c. inputs proportional to the levels of the received signals of the two receivers. The circuit has been arranged to produce outputs of opposite polarity from V10a and V10b which are fed to cathode followers V11a and V11b respectively. The cathode follower outputs are used to bias clamp diodes MR5 and MR6. For equal inputs, the outputs from V10a and V10b are +15V and -15V respectively. However, under conditions of single receiver working only V10a receives an input and, as this is negative, the anode current decreases resulting in an increase in anode potential which is an increase in V10a output. At the same time, the decreased current in R72 common cathode load will decrease the cathode/grid potential of V10b causing a decrease in anode potential and the output goes more negative, i.e. V10a output will be greater than +15V and V10b output will increase negatively by a corresponding amount.

291. When the input level to V10a exceeds the input level to V10b by more than 10dB, V10a is cut off by the signal and V10b is fully conducting. Under these conditions, which are the conditions for single receiver working, the outputs to V11 are +30V and -30V and the clamp diodes are biased at these levels. Thus the telegraph

signal at V14a is clamped at levels of +30V and -30V, but since the signal is already at these levels, the comparator stages have very little effect on single receiver performance.

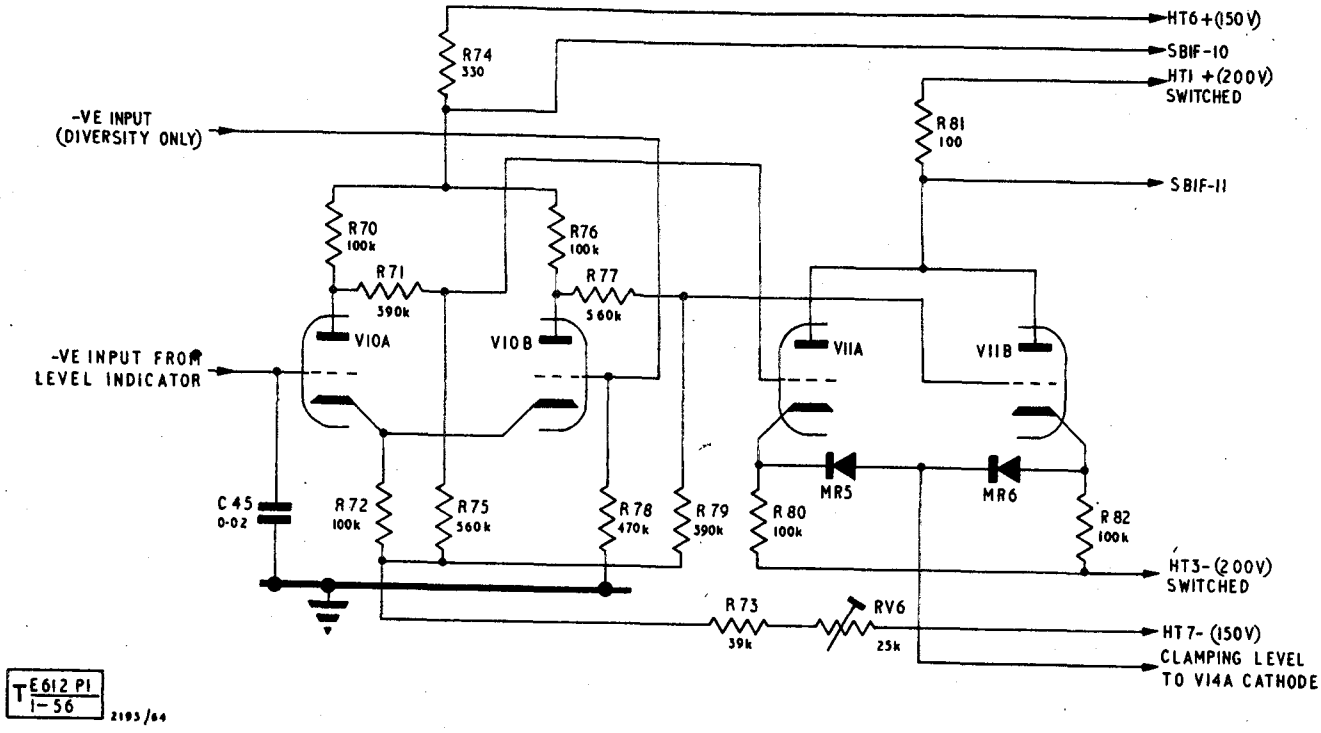

Fig 56 - Comparator stages, circuit diagram

Telegraph a.g.c. circuit V23, V21b

292. The feed to the a.g.c. amplifier (Fig 57) for f.s.k. reception and calibration is taken from the secondary winding of T8 in the i.f.2 amplifier. V23 amplifies the signal which is then developed across L14 and C86 tuned to 100kc/s. C85 couples the signal to rectifier, V21b.

293. A delay voltage of approximately 7.2V, derived from potentiometer chain R185 and R187 across the HT1 line, is applied to V21b cathode.

294. The rectifier output is filtered by R186 and C88 and then taken to the system switch for selection as required.

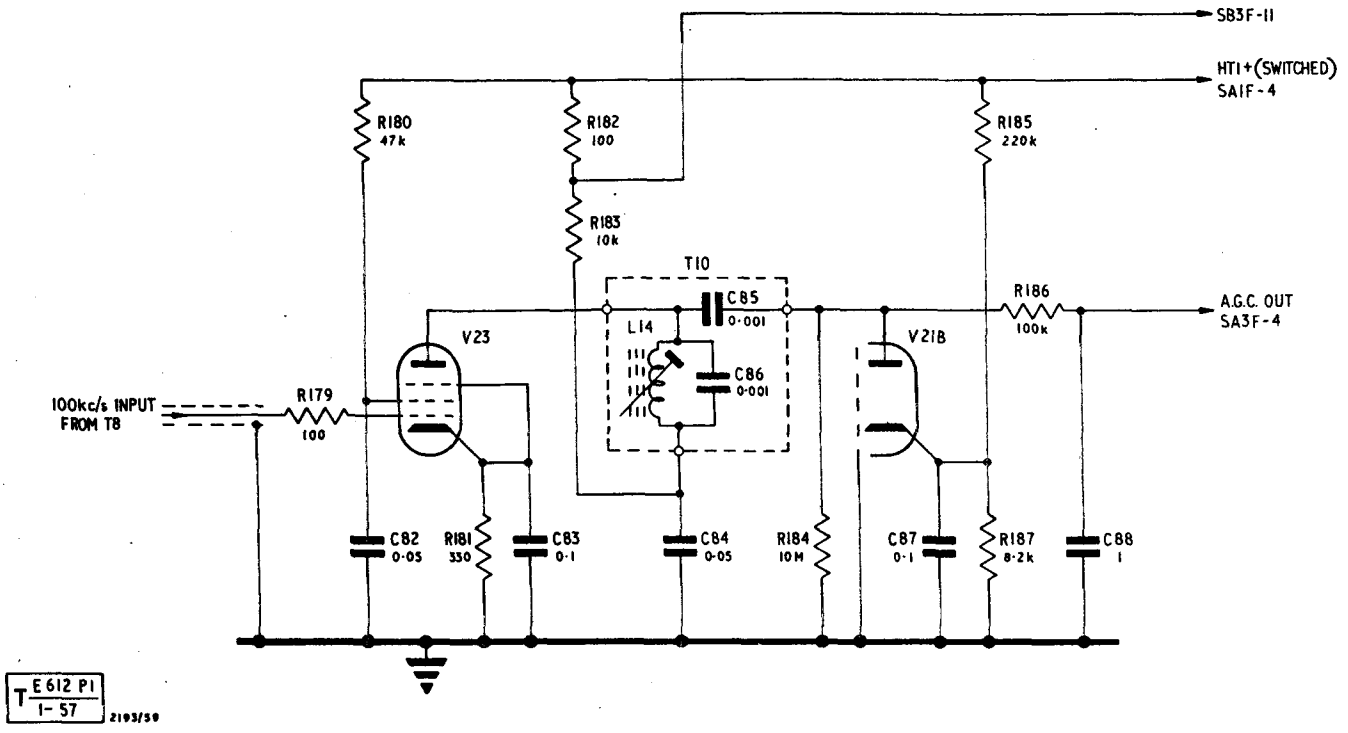

Fig 57 - A.G.C. amplifier and rectifier, circuit diagram

Receiver a.g.c., manual gain control and desensitizing system

295. Fig 58 shows the complete receiver automatic and manual gain control system, and the desensitizing circuit. Cathode follower V2b is included in the system to prevent interaction between the manual gain control circuits when the a.g.c. outputs are combined in a dual diversity station.

296. Telephony a.g.c. voltage is fed from the s.s.b. unit to the telegraph unit for selection by system switch, SA. Telegraphy a.g.c. voltage is also connected to SA, and the selected control voltage is returned to the time constant selecting switch SE mounted on the s.s.b. unit front panel.

297. In the OFF position of SE, the control voltage is connected to earth by R118 and C86 is discharged by R116. At SHORT, SE connects the control voltage to V2b, to R196 and to C86 via the 10MΩ resistor R117 which provides a maintaining current for the 50μF Tantalum capacitor. At LONG, SE connects C86 across the control voltage which is applied to V2b and R196 as before. SE position COMB is used only in dual diversity working when time constant selection is made external to the receiver. Table 15 lists a.g.c. circuit time constants.

Table 15 - A.G.C. time constants

	Short	Long
Charge	4mS	2S
Discharge	50mS	25S

298. RV4 front panel mounted RF GAIN control forms part of a potentiometer chain connected across the HT7 supply rails. The voltage tapped off this chain by RV4 slider is applied to the a.g.c. line via RLA1 contacts and R31 (RLA not energized). A.G.C. output from V2b cathode is also supplied to the a.g.c. line, and the combined control voltage is fed to the s.f. amplifier and to the two i.f.1 amplifiers in the s.f. and i.f.1 unit. MR1 prevents the a.g.c. line being taken positive with respect to earth by V2b cathode current when RV4 is at maximum gain position and there is no a.g.c. input to V2b grid.

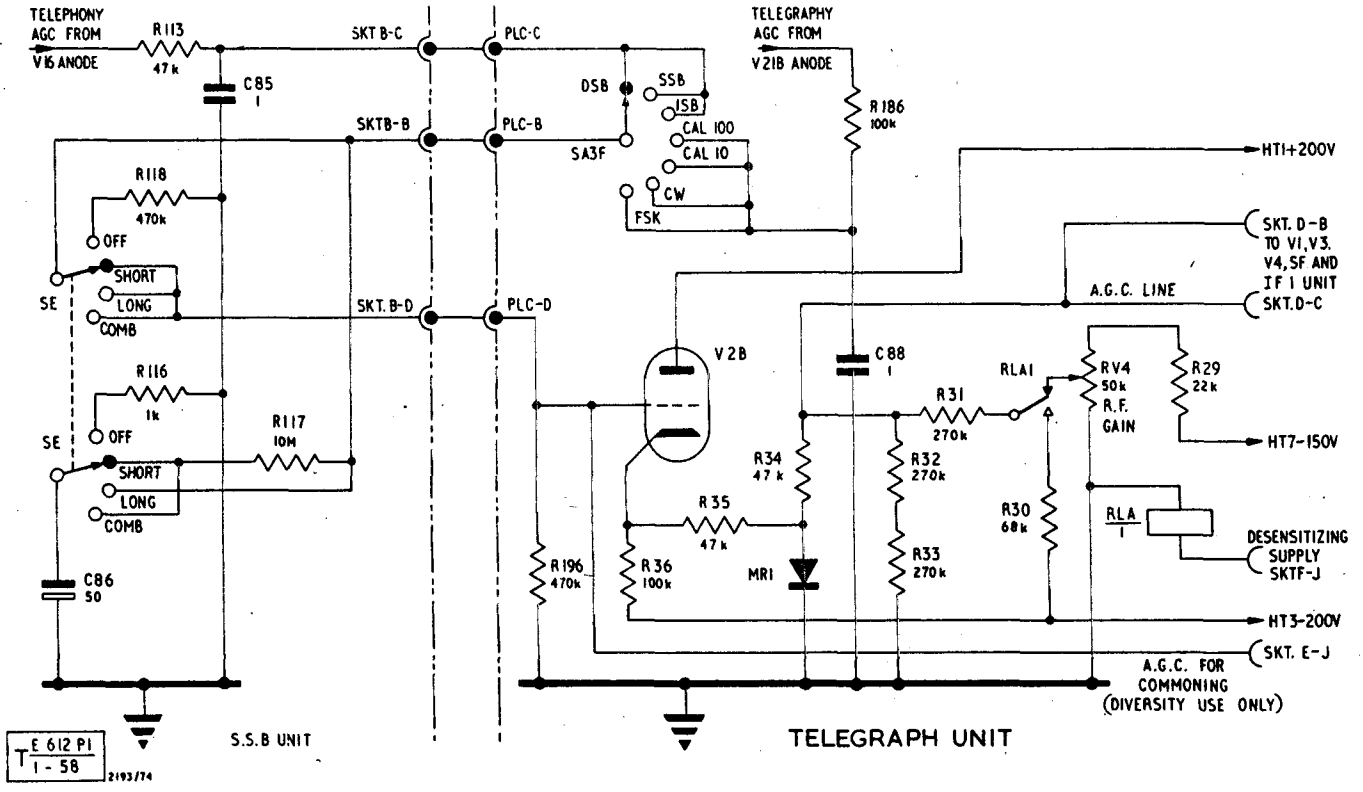

Fig 58 - A.G.C. manual gain control and desensitizing, circuit diagram

299. When RLA is energized, the bias from RV4 is removed and a desensitizing bias of approximately -40V from potentiometer chain R30-R33 across HT3 supply, is applied in its place. For details of relay energizing circuit, see para 304.

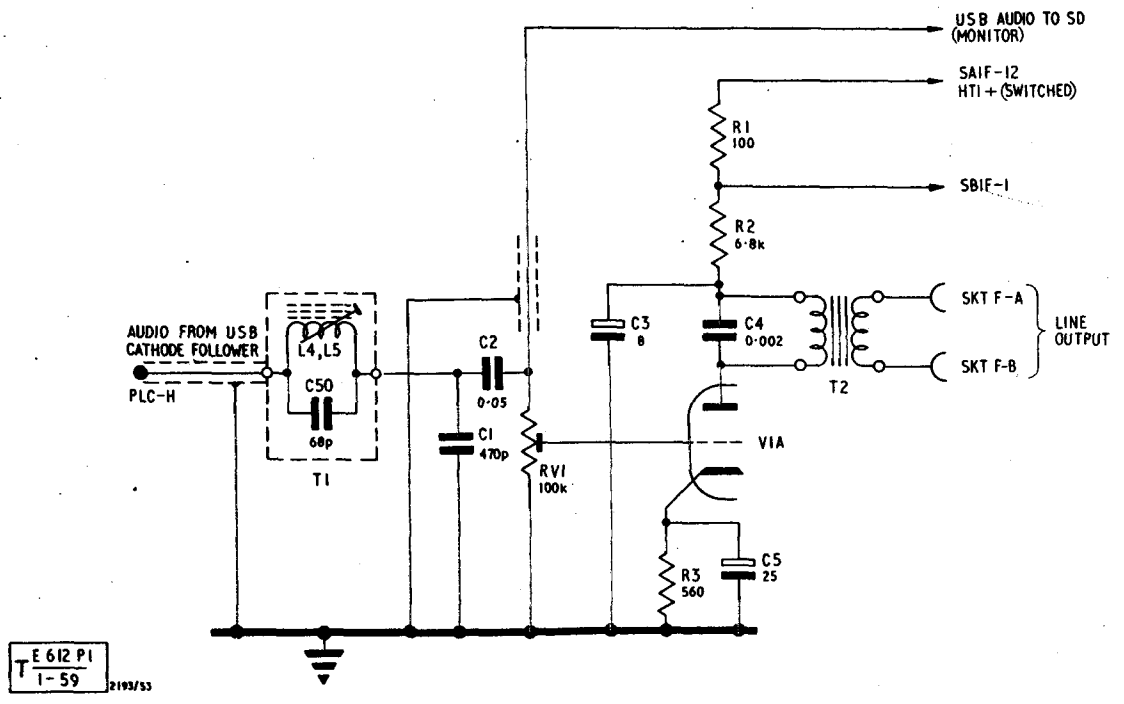

Fig 59 - U.S.B. line amplifier, circuit diagram

Line amplifiers

300. The u.s.b. and l.s.b. line amplifier circuits are identical. The circuit of the u.s.b. amplifier is shown in Fig 59.

301. The u.s.b. audio signal from V5 u.s.b. cathode follower in the s.s.b. unit is fed to V1a grid via T1, C2 and RV1. L4, L5 and C50 in T1 form a rejector circuit tuned to 100kc/s to remove any residual component of the second i.f. from the input signal. RV1, preset u.s.b. gain control, determines the signal input level to V1a. The audio input is also applied to SD MON switch.

302. The output impedance of T2 is 600Ω and the transformer secondary is connected to line via the receiver distribution unit and the control indicator.

System switching

303. The functions of the seven wafer seven position system switch are shown in simplified form in Fig 60 and 61.

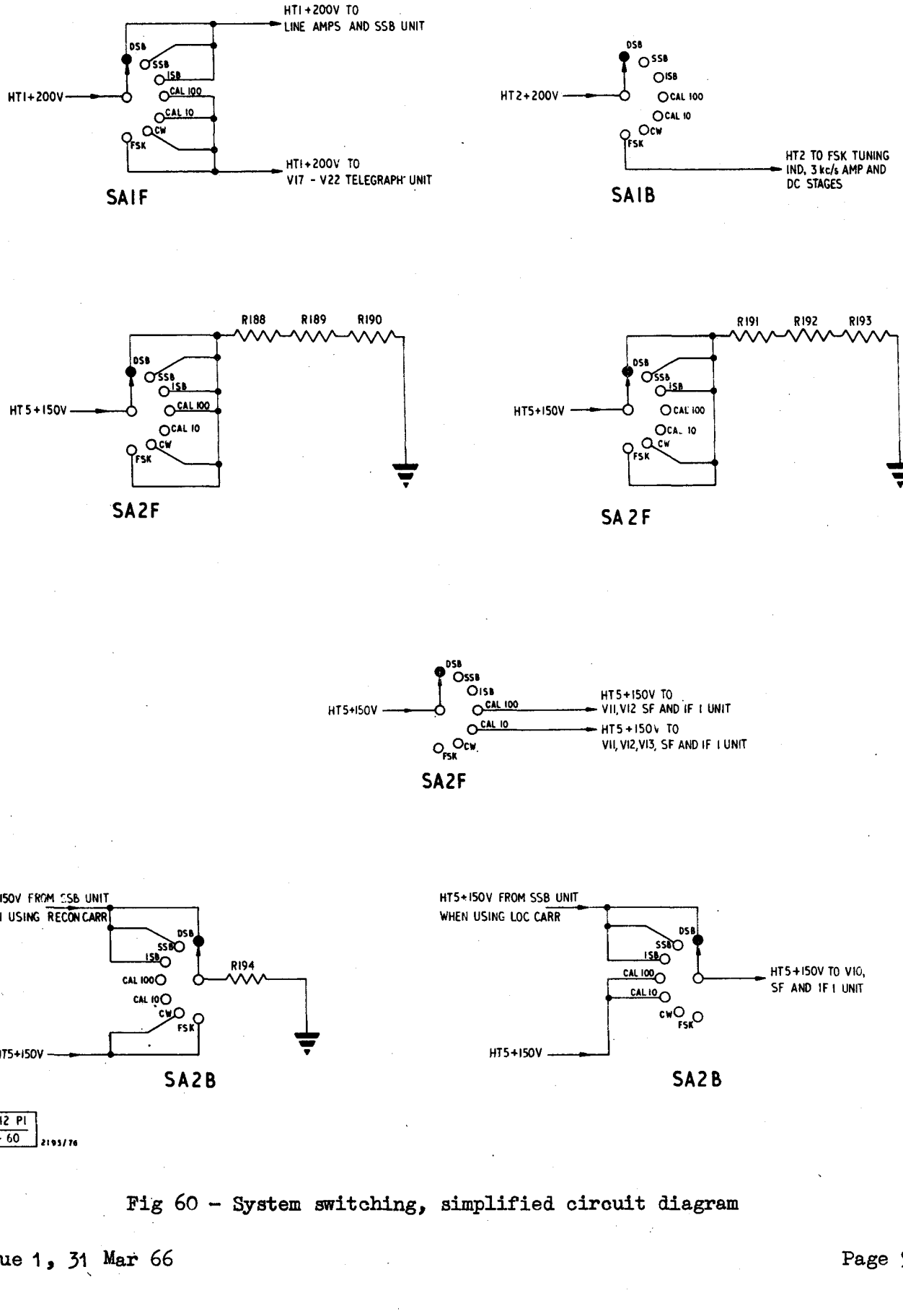

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Fig 60 - System switching, simplified circuit diagram

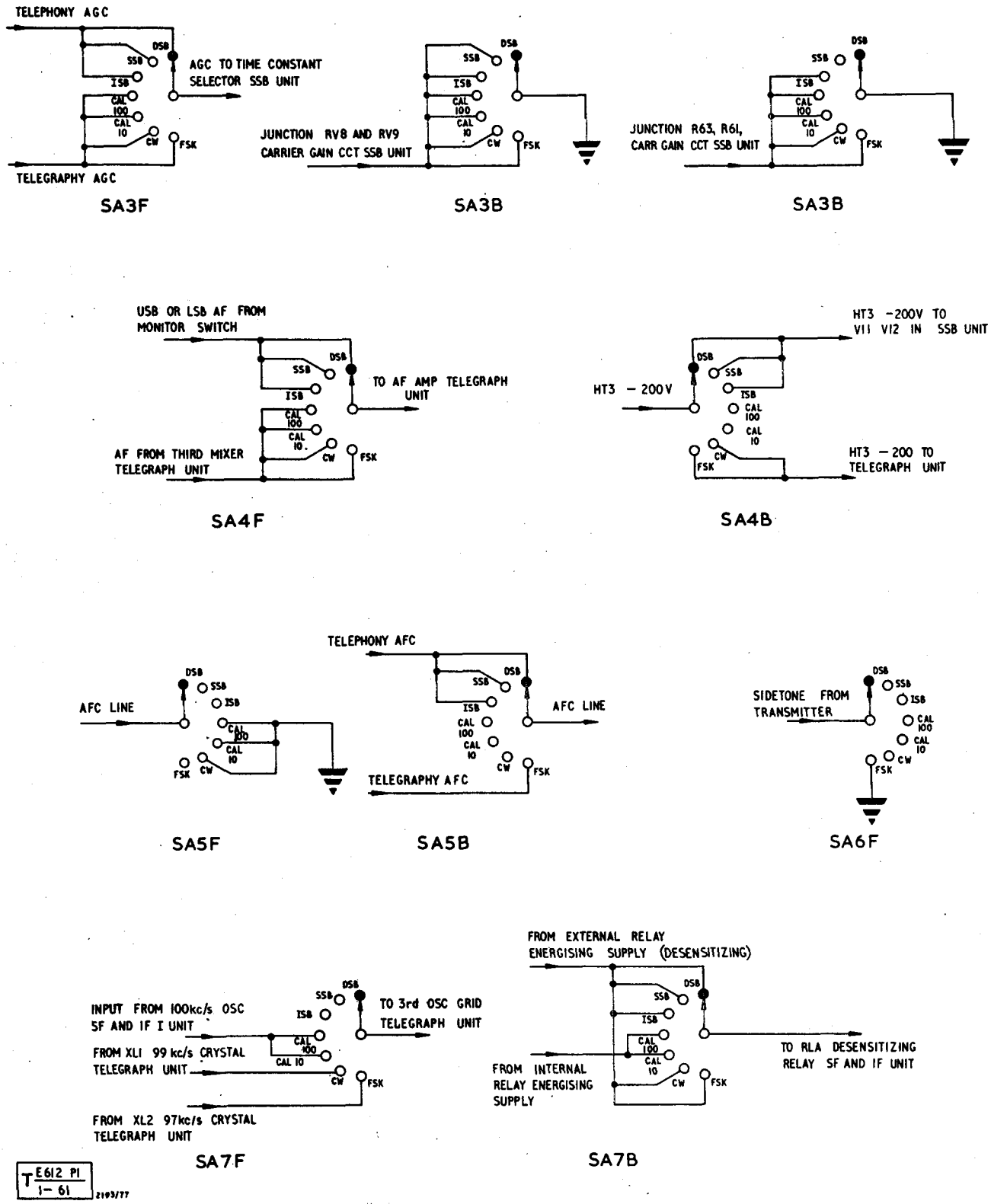

Fig 61 - System switching, simplified circuit diagram

Relay operation, external (desensitizing) and internal energizing supplies

304. Fig 62 is a simplified circuit of the energizing supplies for the receiver relays.

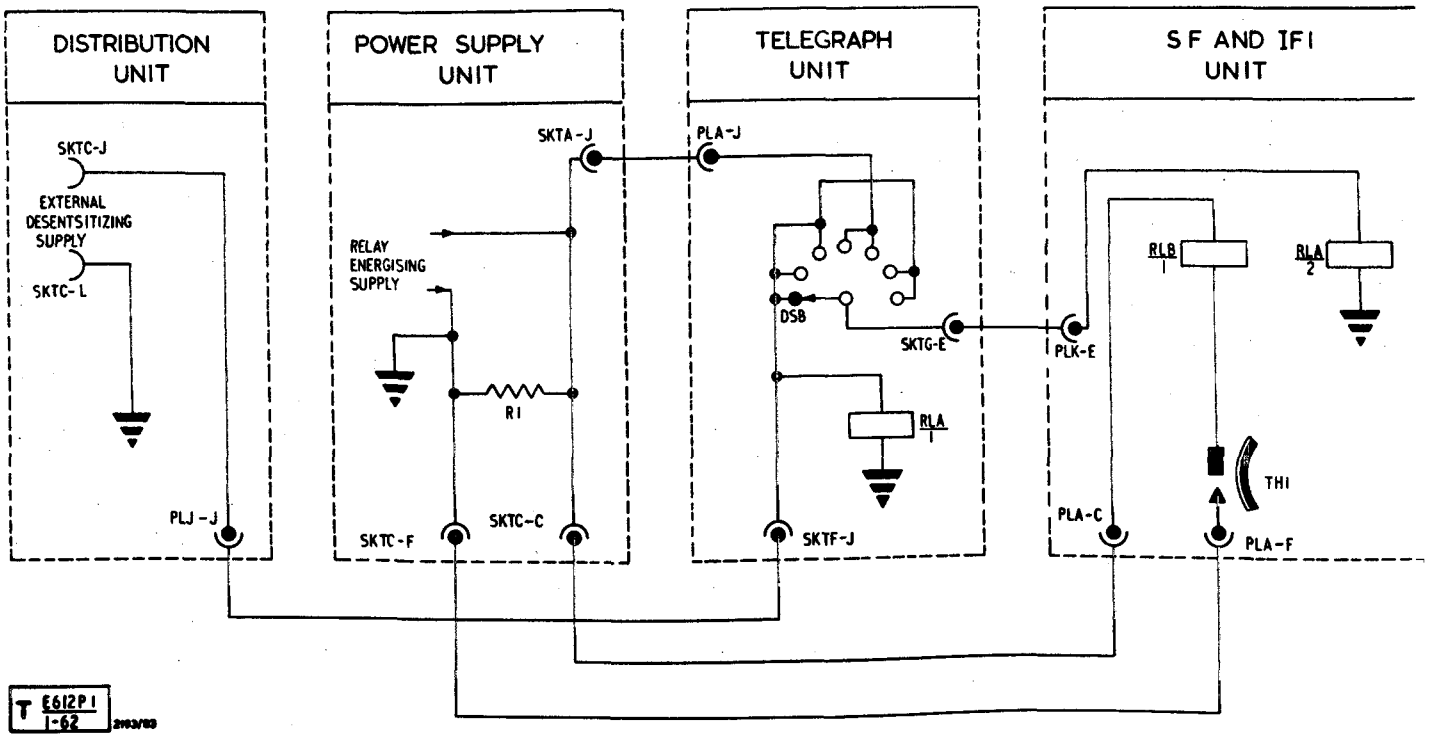

Fig 62 - Relay operation, external (desensitizing) and internal energizing supplies

305. The external desensitizing relay supply is taken from the transmitter on all types of transmission except c.w., and fed to the receiver distribution unit via the control indicator. When working c.w. a separate 24V supply, contained in the control indicator and controlled by the hand key, is used.

306. Operation of the transmitter energizes RLA in the telegraph unit and RLA in the s.f. and i.f.1 unit.

307. In the telegraph unit, relay action disconnects the manual/gain control bias from the a.g.c. line and connects the 40V negative desensitizing bias in its place.

308. In the s.f. and i.f.1 unit, relay action switches the receiver input circuit from antenna to calibrator output, at the same time earthing the antenna input.

309. In the CAL 100 or CAL 10 position of the system switch the receiver internal relay energizing supply in the power supply unit is switched to operate RLA in the s.f. and i.f.1 unit.

310. The internal relay supply is also used to operate crystal oven heater relay RLB in the s.f. and i.f.1 unit.

Monitoring facilities

311. Current monitoring resistors are included in the anode circuits of all valves except diodes V8 and V21. Anode current selection for monitoring by M2 is carried out by METER switches SB and SC. In the RELAY position SC switches M2 across R134 to measure telegraph relay current. In addition, M2 acts as a tuning indicator on telephony or f.s.k. reception as selected by SC.

312. M1 indicates the level of the received signal when working f.s.k.

Supplies

H.T.

313. H.T.1 (+200V), H.T.2 (+200V), H.T.3 (-200V), H.T.6 (+150V) and H.T.7 (-150V) supplies are all utilized by the telegraph unit.

314. The H.T.1 and H.T.3 supplies are inter-connected by a series of resistors in the s.s.b. unit. MR9 is included in the h.t. circuit in the telegraph unit to protect the electrolytic capacitors against damage by the application of incorrectly polarized voltage in the event of removal of the H.T.1 supply.

315. The H.T.2 and H.T.3 supplies are inter-connected by a series of resistors in the d.c. amplifying stages in the telegraph unit and MR10 is included across the H.T.2 supply rails to afford electrolytic protection in the event of removal of the positive supply.

L.T.

316. V3 has a 6.0V heater which is fed from the LT4 supply.

317. All other valves in the unit have either 6.3V heaters or 12.6V centre tapped heaters with the two halves parallel connected.

318. The heaters are connected in parallel and split into four groups for connection to the L.T.1 supply at PLA. One side of each group is earthed.

POWER SUPPLY UNIT, TYPE 7554A
(incorporating Power Supply Unit Type 5441A)
(Fig 2521-2526)

General

319. The power supply unit provides all the a.c. and d.c. supplies required by the receiver.

320. A general view of the unit is shown in Fig 63. Major components are mounted on the top of the chassis deck with cut-outs to permit transformer, inductor and capacitor terminals to protrude through to the underside of the deck for ease of wiring. Further cut-outs assist ventilation. Small components are mounted on tagboards fixed to the top and underside of the chassis.

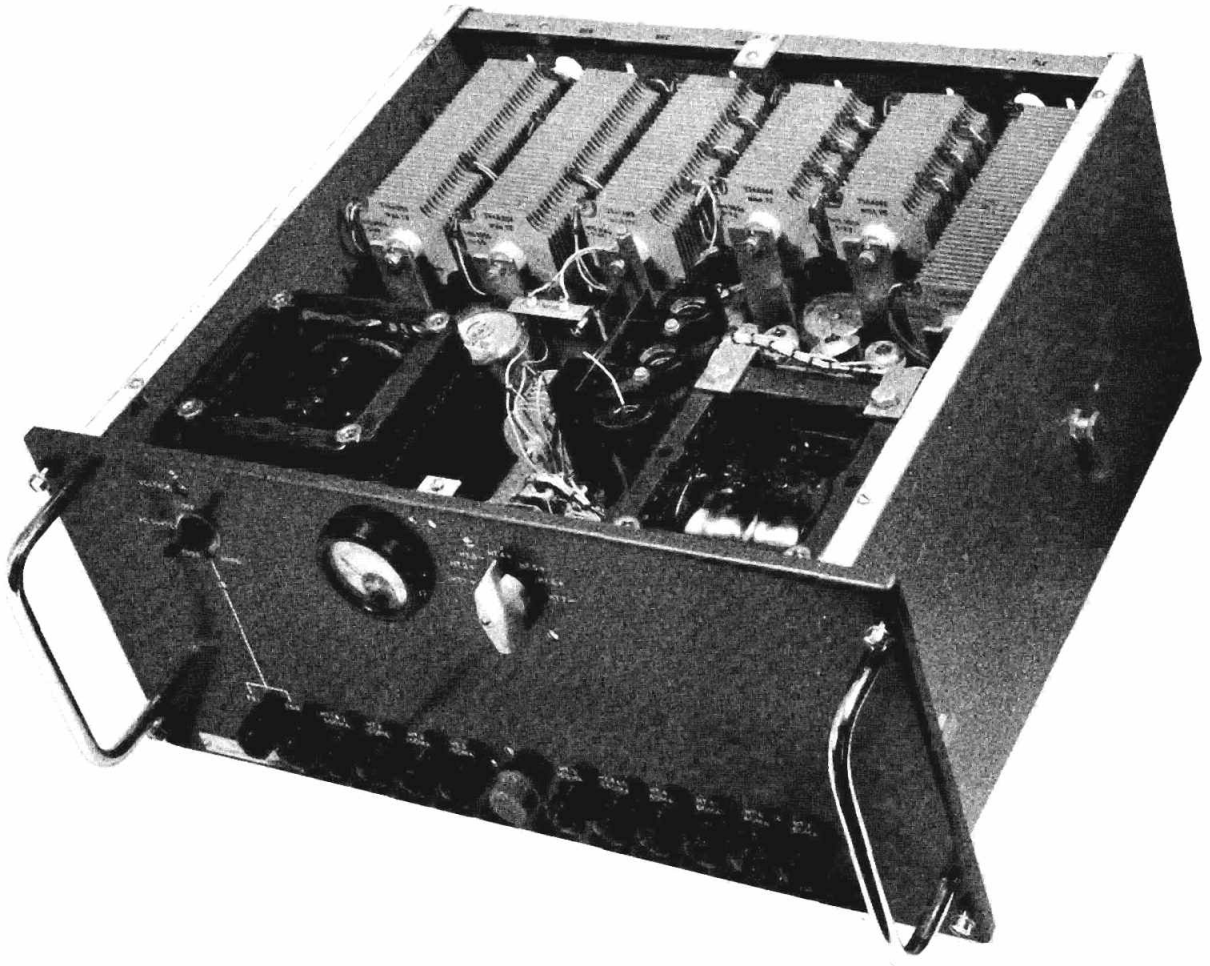

Fig 63 - Power supply unit, general view

321. Two multi-winding mains transformers are used, one of which (T2, right) in conjunction with selenium rectifiers and smoothing circuits, provides seven h.t. supplies. The other transformer (T1, left) provides five l.t. supplies and a.c. inputs for the relay energizing supply, the oven heater and supply unit type 5441A.

322. The Power Supply Unit, Type 5441A, can be seen mounted on a sub-chassis located on top of the main chassis between the two mains transformers.

323. The front panel accommodates all fuses, the on indicating lamp, h.t. supply monitoring facilities, the A.C. SUPPLY on/off switch and the mains input voltage indicating disc which is viewed through a window adjacent to the switch. Table 4 gives full details of front panel component functions.

Input circuit

324. A simplified block diagram of the power supply unit is shown at Fig 64.

325. The two mains transformers, T1 and T2, both possess split tapped primary windings. The two sections of each primary can be interconnected in series or in parallel to enable the unit to operate on mains supplies of 100-130V a.c. or 200-250V a.c., 45-65c/s single phase. The tappings on each primary must be separately adjusted for the mains voltage available, and the front panel voltage indicating disc set accordingly. Fig 2524 shows the correct primary connections for the full range of operating voltages.

326. The mains input enters the unit at PLE, is double fused by FS1 and FS2 and controlled by SA double pole on/off switch before being applied to T1 and T2 primary windings.

Transformer T1 and l.t. circuits

327. T1 has seven secondary windings, 'c', 'd', 'e', 'f', 'g', 'h' and 'j'. These provide the following L.T. supplies:

Winding 'c'. Provides LT1 supply of 7V, 7A (nominal 6.3V fully loaded) for all the heaters of the telegraph unit valves, excluding V3.

Winding 'd'. Provides LT2 supply of 7V, 3.5A (nominal 6.3V when fully loaded) for the heaters of V1 to V6 inclusive, V9 to V12 inclusive and V14 and V15 in the s.f. and i.f.1 unit.

Winding 'e'. Provides LT3 supply of 7V, 7A (nominal 6.3V when loaded) for the heaters of all valves in the s.s.b. unit. The on lamp ILP1, which indicates that l.t. supplies for all circuits are available, is connected across this winding.

Winding 'f'. Provides LT4 supply of 6.4V, 0.75A (nominal 6.3V on load) for the 6V heater of V3 in the telegraph unit.

Winding 'g'. Provides 21V, 0.6A input for the 12.6V d.c. stabilized power supply unit, type 5441A.

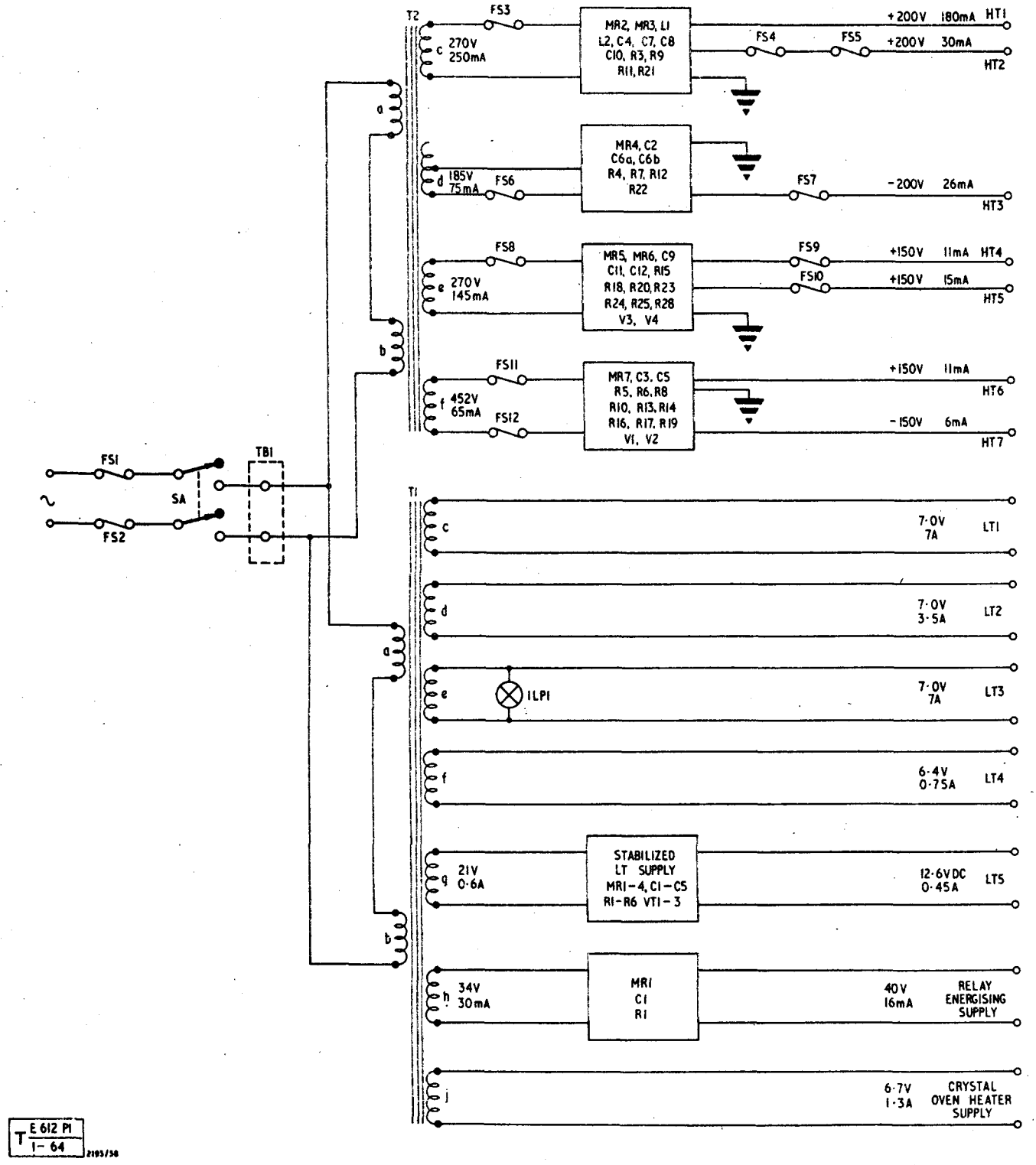

Fig 64 - Power supply unit, simplified block diagram

Winding 'h'. Provides 34V, 30mA to the rectifying circuit of the relay operating supply.

Winding 'j'. Provides 6.7V, 1.3A (nominal 6.6V on load) for the heater of the crystal oven.

Transformer T2 and h.t. circuits

328. Transformer T2 has four secondary windings from which are derived seven h.t. supplies as follows:

H.T.1 +200V, 180mA d.c. for the s.f. and i.f.1, s.s.b. and telegraph units.

H.T.2 +200V, 30mA d.c. for the telegraph Unit (f.s.k. circuits). HT1 and HT2 supplies are obtained from winding 'c' which feeds two full-wave selenium rectifiers MR2, MR3 connected as a bridge. The a.c. input to the bridge is fused by FS3 (500mA) and the h.t.1 output is smoothed by the two-section choke input filter L1, C8, L2, C10 with bleeder resistor R21. The h.t.2 supply is smoothed by the first section L1, C8 of the choke input filter and fused by FS4 (150mA anti-surge). Further smoothing is provided by the resistance-capacitance filter R3, C4, R11 and C7 with bleeder resistor R9, and fused by FS5 (150mA).

H.T.3 -200V, 26mA d.c. for the telegraph Unit and s.s.b. Unit. This is obtained from winding 'd', a centre-tapped winding of which only half is used to feed the selenium bridge rectifier MR4. The a.c. input to the bridge is fused by FS6 (150mA anti-surge). The output is smoothed by the resistance-capacitance filter C2, R12, C6A and C6B with bleeder resistors R7 and R22 and is fused by FS7 (150mA). R4 in the output arm of the bridge is a peak current limiter.

H.T.4 +150V, 11mA, stabilized for the reactance valve and second oscillator valves in the s.f. and i.f.1 unit.

H.T.5 +150V, 15mA, stabilized for the calibrator valves in the s.f. and i.f.1 unit.

HT4 and HT5 supplies are derived from winding 'e' which provides 270V, 145mA for two selenium bridge rectifiers MR5 and MR6 in parallel. The a.c. feed to the rectifiers is fused by FS8 (250mA anti-surge). R15 in the output arm of the bridge is a peak current limiter. C9 is the common reservoir capacitor and smoothing for the HT4 supply is provided by R23 and C12 and the output, fused by FS9 (60mA) is fed to the stabilizing circuit comprising the current limiting resistor R25 and the neon stabilizer V4. The stabilized output is partly loaded by R28 connected across V4. For the HT5 supply smoothing is provided by R20 and C11 and the output, fused by FS10 (60mA), is fed to the stabilizing circuit comprising the current limiting resistor R24 and the neon stabilizer V3.

H.T.6 +150V, 11mA, stabilized for the comparator, clamp, a.f.c. comparator and discriminator circuits in the telegraph unit.

H.T. 7 -150V, 6mA, stabilized for the crystal calibrator in the s.f. and i.f.1 unit and for the comparator, clamp and a.f.c. comparator circuits in the telegraph unit.

HT6 and HT7 supplies are derived from winding 'f' which provides 227-0-227V, 65mA to the selenium bridge rectifier MR7. The a.c. input to the bridge is fused by FS11 (150mA anti-surge) and FS12 (150mA anti-surge) and the output circuit is balanced about earth to provide two outputs. The positive output of the bridge from reservoir capacitor C5, with bleeder resistor R10 in parallel, is applied to the stabilizing circuit comprising current limiting resistors R13 and R17 in series and neon stabilizer V2. The negative output of the bridge from reservoir capacitor C3 with bleeder R8 in parallel is applied to the stabilizing circuit comprising the series connected current limiting resistors R14 and R16 and the neon stabilizer V1. The stabilized output is partly loaded by R19 connected across V1. R5 and R6 in the output arms of the bridge are current limiters.

Monitoring facilities

329. All h.t. supplies are monitored by the 1mA f.s.d. moving-coil meter M1 which is connected between each h.t. supply and earth by switch wafers SB1 and SB2. R26 and R27 are the meter multipliers.

Power Supply Unit, Type 5441A

330. The power supply unit, type 5441A, is a transistorized unit supplying a stabilized output of 12.6V d.c. at 0.45A for the heaters of the second oscillator, 10kc/s multivibrator and reactance valves in the s.f. and i.f.1 unit.

331. Some of the main components of the unit, located between the mains transformers can be seen in Fig 63. Large capacitors, C1, C2 and C3, isolated from earth, are mounted on the right of the unit sub-chassis. On their left is VT1 heat sink and MR1. The circuit diagram is given in Fig 65.

332. Winding 'g' of TR1 supplies 21V a.c., to the regulated supply unit. This comprises the conventional bridge rectifier MR1 with reservoir capacitor C1 followed by the regulating circuits. These consists of the series regulator VT1, the control transistor VT3 (the error amplifier) Zener diode MR4, which provides a reference voltage for the emitter of VT3, and the series regulator driver transistor VT2, which matches the output impedance of VT3 and the input impedance of VT1. The collector supply for the control transistor VT3 is obtained from germanium diodes MR2 and MR3, fed in parallel with the bridge rectifier, and reservoir capacitor C2.

333. VT3 is a common emitter stage with its emitter potential held constant by the reference diode MR4. VT1 and VT2 form a compound emitter follower consisting of two emitter followers directly coupled in cascade. Regulation is effected by applying d.c. feedback from output to series regulator, the d.c. feedback loop extending from the output via the potentiometer chain, R4, RV1 and R5, to the base of VT3, thence from VT3 collector to the base of VT2 and from the emitter of VT2 to the base of VT1.

334. Any change in the output voltage gives rise to a corresponding change in the voltage applied to VT3 base. The amplified changes in VT3 collector current are

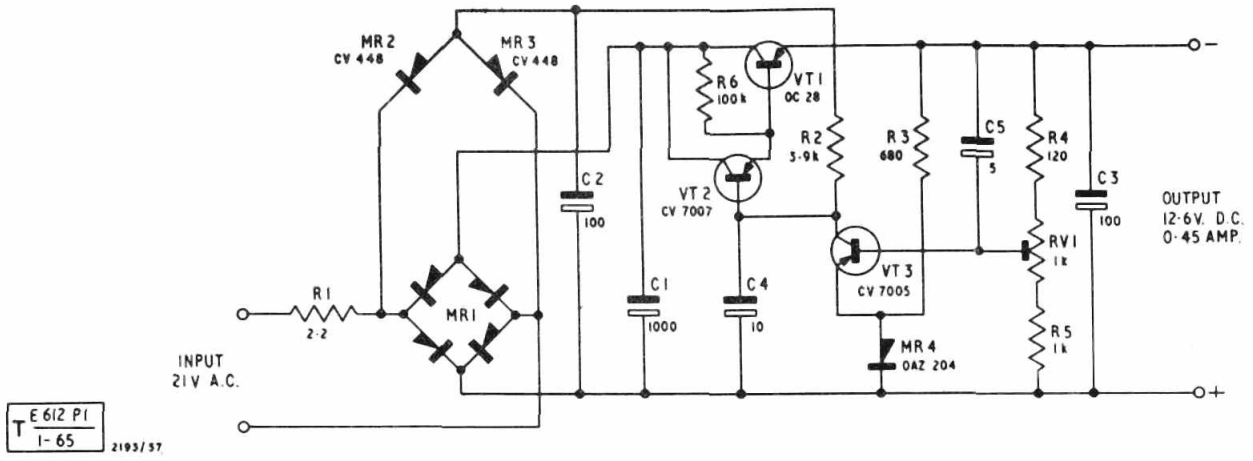

Fig 65 - Power supply unit, stabilized power supply circuit diagram

applied to the base of the driver VT2. This stage and VT1, the series regulator, are cascaded common collector (emitter follower) stages and the effect of the d.c. feedback is to vary the effective resistance of VT1 so that the output voltage tends to remain constant. VT1 and VT2 are connected in cascade to effect a greater reduction in output impedance than that obtainable with one emitter follower stage. RV1 controls the output voltage and this control is located at the front end of the sub-chassis, just behind the front panel of the main unit, and is accessible from the top.

DISTRIBUTION UNIT, TYPE 5417A
(Fig 2527-2529)

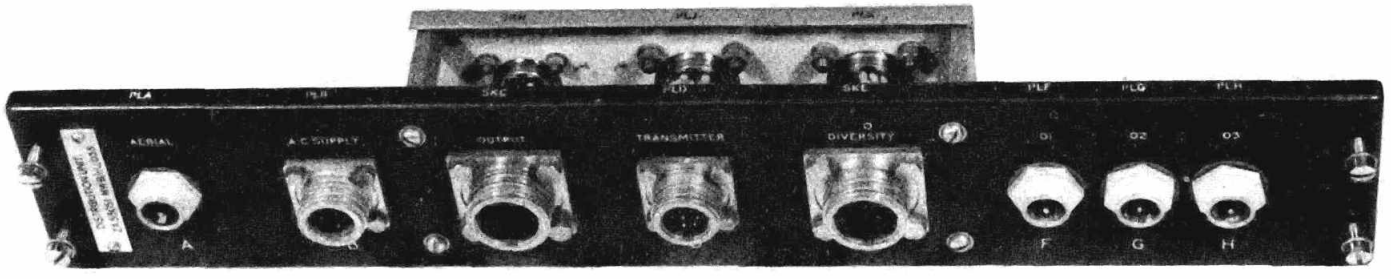

Fig 66 - Distribution unit, general view

General

335. Fig 66 is a general view of the distribution unit. The front panel is secured to the bottom front of the cabinet by four captive screws and the backplate is attached to four pillars which are screwed to the front panel.

336. All external connections to the receiver are made to the front panel of the unit, including the antenna feeder and the co-axial leads inter-connecting the oscillator stages of two receivers working in dual diversity.

337. The Mk 4B plugs and sockets on the panel are connected to the Mk 4B plugs and socket on the backplate, which in turn are connected to the telegraph and power supply units by the internal receiver cable harness (Fig 2531). The co-axial plugs are coupled to the s.f. and i.f.1 unit by co-axial leads in the cable harness.

338. Table 5 details plug and socket functions.

EME80/2193

END of Part 1