RECEIVER TYPE RA.2091C

Ref. WOH 6245
Issue A, 9.76-100

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CHAPTER 1

TECHNICAL DESCRIPTION

OVERALL RECEIVER UNIT AND POWER SUPPLIES

INTRODUCTION

1. The purpose of this chapter is to present the interconnecting information for the Receiver unit, and to describe the Receiver main power supplies. Chapters 2 to 4 describe in detail the main receiver functions viz. the tuning system, the synthesizer and the i.f. processing stages. The depth of servicing covered by this publication entails fault-location to sub-assembly level (printed-wirng board) and its replacement. The depth of the technical descriptions (Chap. 1 to 4) is defined by the above servicing policy and hence restricted to the following:-

(a) Specifying the input and output levels, where possible, on each printed-wiring board.

(b) Defining the function of all semi-conductor devices (if not self-evident).

These chapters have also been prepared to serve as an aid to fault finding, and appropriate cross-reference will appear in Chap. 5 (Fault Finding).

INTERCONNECTIONS

2. Figure 37 is the interconnection diagram for the complete receiver unit. A comparison with figures 2, 3 and 4 (Operator's Manual) will reveal the functions carried out by each printed-wiring board. It will be necessary to refer to the interconnection diagram when reading Chap. 2 to 4.

POWER SUPPLY

3. The power supply (fig. 3) consists of a printed-wiring board and a number of off-board components forming one removable assembly; the main voltage selector is mounted on the rear panel of the receiver. The power supply produces a number of d.c. supplies rated as follows:

(a) +8V to +10V at 1.2A, unregulated

(b) +5V at 0.6A, regulated

(c) +20V at 100 mA regulated

(d) +35V at 20 mA, regulated

(e) +12V at 1A, regulated

(f) -12V at 200 mA, regulated

(g) +12V at 200 mA, unregulated

4. With reference to fig. 37, mains voltage is applied via the three-position POWER switch to the power supply assembly. In the STBY (Standby) position of the POWER switch, a built-in battery provides power for the logic board to maintain the memory; refer to Chap. 3 for a description of the battery-standby supply. Mains voltage is not applied to the power supply assembly until the POWER switch is set to ON.

CHAPTER 2

TECHNICAL DESCRIPTION

RECEIVER I.F. PROCESSING

INTRODUCTION

1. The receiver i.f. processing is carried out in the following printed-wiring boards; refer to fig. 37 for board interconnections.

   (1) 2nd Mixer and I.F. Filter board.

   (2) I.F. Amplifier board.

   (3) F.M./C.W. Detector board.

   (4) B.F.O. board.

This chapter also describes the Video and Audio Amplifier board and the C.O.R./SER. Control board.

2nd MIXER AND I.F. FILTER BOARD (fig. 5)

2. The 1st i.f. signal input from the R.F. Tuner Head is mixed with the 2nd local oscillator output to produce the 2nd i.f. signal (Table 1). The mixer output, containing a band of frequencies centred upon 21.4 MHz, is fed to a three-stage tuned amplifier having an overall gain of 18 dB; the gain is controlled by the AGC2 input to pin 8 of the board (para. 11).

TABLE 1

2nd Mixer: Signal Frequencies (MHz)

Receiver Range	1st I.F.	2nd L.O.	2nd I.F.
19.499 - 40.499	122	143.4	21.4
39.499 - 90.499	122	143.4	21.4
89.499 - 195.499	72	93.4	21.4
194.499 - 400.499	122	143.4	21.4
399.499 - 650.499	122	143.4	21.4
649.499 - 999.499	122	143.4	21.4

3. The amplified signals are fed to the inputs of four band-pass filters. The selected filter output, as determined by the setting of the IF BANDWIDTH-kHz switch, is passed to the output amplifier stage and thence to the I.F. Amplifier board; the stage gain of the output amplifier is controlled by the AGC 1 input to pin 15 of the board.

4. The amplified i.f. signal is also fed, prior to the filtering, to a buffer amplifier stage and thence to a Spectrum Display Unit via IF output 1 (Part 2).

5. The functions of all the semiconductor devices on the board are given in Table 2.

TABLE 2

2nd Mixer and I.F. Filter Board: Semiconductor Functions

Semiconductor	Function
X1	Mixer
TR2-4, TR8, TR12-14	I.F. Amplifier
D14	AGC-2, PIN attenuator
1C1	I.F. Output stage
TR1	S.D.U. Output stage
TR5, D2, D3, D4	Select 50 kHz Filter
TR9, D5, D6, D7	Select 6 kHz Filter
TR10, D8, D9, D10	Select 20 kHz Filter
TR11, D11, D12, D13	Select 300 kHz Filter

6. The control potentials for i.f. filter selection are given in Table 3. The D.C. supply voltages are given in fig. 5.

TABLE 3

2nd Mixer and Filter Board: I.F. Bandwidth Selection

Mode	Pin	I.F. Bandwidth (kHz)			
		6	20	50	300
		See Notes			
CW	14			X	
	12		X		
	10	X			
	9				X
	7	X	X	X	X
	6	X	X	X	X
	5	X	X	X	X
AM	14			X	
	12		X		
	10	X			
	9				X
	7	X			
	6				
	5		X	X	
FM	14			X	
	12		X		
	10	X			
	9				X
	7	X			
	6				
	5		X	X	

TABLE 3 (Cont'd)

Mode	Pin	I.F. Bandwidth (kHz)			
		6	20	50	300
PULSE	14			X	
	12		X		
	10	X			
	9			X	
	7	X			
	6				
	5		X	X	

Notes:
1. X denotes +11V (nominal) control level.
2. +11V on pin 9 activates the 22 MHz oscillator.
3. +11V on pin 11 activates the 16.65 MHz oscillator.

I.F. AMPLIFIER BOARD (fig. 7)

7. The 21.4 MHz input, from the 2nd Mixer and I.F. Filter board, is fed to a three-stage amplifier having an overall gain of 66 dB; the gain of the first stage is set by either the manual IF GAIN or the a.g.c. circuits (para. 11). The amplified signals are fed to the F.M./C.W. Detector board (para. 14).

8. The amplified i.f. signal is also fed to the a.m./a.g.c. detector. The resultant audio signals are passed to a buffer stage and thence to the F.M./C.W. Detector board at a signal level of 50 mV r.m.s. The audio output is muted when a +12V input from the MODE switch is applied to pin 1 of the board.

9. A portion of the signal at the second amplifier stage is fed to the c.w. detector (para. 19).

10. The output from the first amplifier stage is also fed to a separate two-stage amplifier to provide the I.F. No. 2 output (signal level 25 mV minimum).

11. An a.g.c. potential is developed at the a.m./a.g.c. detector and fed via buffer amplifiers to the a.g.c. time-constant circuits; as determined by the MODE switch setting, a +12V input to pin 8, 4 or 3 of the board selects the desired time-constant. The a.g.c. potential or a d.c. input to pin 5 - from the IF GAIN control - is then fed to a further amplifier stage which produces the AGC2 output (pin 13); selection of automatic or

manual gain control is determined by a 12V input. The AGC2 output is fed to the R.F. Tuner Head (Part 3), the 2nd Mixer and Filter board and the C.O.R./Serialiser/Squelch board. The AGC2 voltage is also fed to two separate amplifier stages which in turn provide the following:-

(1) The control potential for the i.f. amplifier (para. 2).

(2) The AGC1 output (pin 2).

(3) The drive to the 'S' meter (pin 11).

12. As the r.f. signal input rises, the gains of the receiver circuits are reduced in the following sequence; a total control range of about 100 dB is provided.

(1) I.F. Amplifier board (30 dB control, internally connected).

(2) R.F. Tuner Head (25 dB control via AGC2).

(3) 2nd mixer and filter board (25 dB control via AGC2).

(4) 2nd mixer and filter board (20 dB control via AGC1).

13. The functions of all the semiconductor devices on the board are given in Table 4.

TABLE 4

I.F. Amplifier Board: Semiconductor Functions

Semiconductor	Function
1C1, 1C2, TR2	I.F. amplifier
1C4, TR4	Output amplifier
D1	A.M./A.G.C. detector
TR3	Audio output and A.G.C. buffer
TR5	Audio muting
IC3	A.G.C. amplifiers
D2	Clamping diode
IC5 (part)	Off-set amplifier
TR1	A.G.C. clamp
IC5 (part)	'S' meter amplifier
TR6, D3	Manual gain control

TABLE 4 (Cont'd)

Semiconductor	Function
TR7	A.G.C. switch
TR8-13, D4, D5	Selection of A.G.C. time-constant
D8, D6	A.G.C. clamp

F.M./C.W. DETECTOR BOARD (fig. 9)

14. Depending upon the setting of the IF BANDWIDTH-kHz switch, f.m. demodulation is carried out in one of three separate discriminators. When the 300 kHz bandwidth is selected (Table 5), the 21.4 MHz i.f. input (terminals 10 and 11) is applied to a f.m. discriminator operating at this frequency.

15. When the 6 kHz bandwidth is in use, the 21.4 MHz input is mixed with the 22 MHz output from the B.F.O. board (para. 22) and then fed to the 6 kHz f.m. detector which operates at 600 kHz. When the 20 kHz or 50 kHz bandwidth is in use, the input signal is mixed with the 16.65 MHz output from the B.F.O. board and demodulation is performed at 4.75 MHz.

16. The video signal, developed by the f.m. discriminator in use, is fed to a buffer amplifier stage. The video output signal level (terminal 17) is 12 mV r.m.s. (minimum).

17. The video output is also fed via a further buffer stage to provide the audio output (pin 4). The audio path is protected by a noise limiter which is controlled by +11V input to pin 2.

18. The drive for the front panel meter (meter switch set to TUNE) is derived from a d.c. output from the f.m. discriminator in use. The meter output, -5V to +5V at pin 3, is disabled in the c.w. mode by the +11V input to pin 5.

19. In the c.w. mode, the i.f. input to terminals 14 and 15 is passed to a buffer amplifier stage and then mixed with the 21.4 MHz variable - b.f.o. signal. The demodulated output is passed to the Video and Audio Amplifier board.

20. The control potentials for signal path selection are given in Table 5. The d.c. supply voltages are given in fig. 9.

TABLE 5

F.M./C.W. Discriminator Board: Control Potentials

Mode	Pin	I.F. Bandwidth (kHz)			
		6	20	50	300
		See Notes			
C.W.	5	X	X	X	X
	8	X			
	9	X			
	10		X		
	11			X	
	12			X	
	13		X		
	14				X
	15				X
A.M.	5				
	8	X			
	9	X			
	10		X		
	11			X	
	12			X	
	13		X		
	14				X
	15				X
F.M.	5				
	8	X			
	9				
	10				
	11				

TABLE 5 (Cont'd)

Mode	Pin	I.F. Bandwidth (kHz)			
		6	20	50	300
F.M. (Contd)	12			X	
	13		X		
	14				
	15				X
PULSE	5				
	8	X			
	9	X			
	10		X		
	11			X	
	12			X	
	13		X		
	14				X
	15				X

Notes:
1. X denotes +11V (nominal) control level
2. +11V at pin 5 selects tuning meter input.
3. +11V at pin 2 activates the noise limiter.

21. The functions of all the semiconductor devices on the board are given in Table 6.

TABLE 6

F.M./C.W. Discriminator Board: Semiconductor Functions

Semiconductor	Function
IC1	Mixer, 6 kHz bandwidth
IC2	F.M. detector, 6 kHz bandwidth
IC3	Buffer Amplifier, high input impedance for tuning meter
IC4	Tuning Meter Amplifier
IC5	Audio and Video pre-amplifiers
IC6	Mixer, 20 kHz and 50 kHz bandwidths
IC7	F.M. detector, 20 kHz and 50 kHz bandwidths
IC8	F.M. detector, 300 kHz bandwidth
IC9	C.W. Mixer
TR1, TR2, TR5-8, D4, D14, D15	Select input to tuning meter
TR3	Tuning Meter output switch
TR4	Noise limiter switch
TR9-13	Audio and video bandwidth and gain tailoring
TR10	C.W. Buffer Amplifier
D1, D2, D7-12, D16 D17, D20, D21	Logic switching: select f.m. detectors
D3, D13, D19	Zener diodes
D5, D6	Noise limiter

B.F.O. BOARD (fig. 11)

22. The B.F.O. board provides three separate outputs - 16.65 MHz, 22 MHz and 21.4 MHz - to the F.M./C.W. Detector board. Two crystal oscillators operate at 16.65 MHz and 22 MHz; the 22 MHz oscillator is varactor-tuned by a d.c. input from the BFO TUNE control.

23. To provide the 21.4 MHz signal, the crystal oscillator outputs are mixed to produce 5.35 MHz. This signal is fed to a frequency-quadrupler stage and, after amplification, provides the b.f.o. output.

24. The signal and control levels for the B.F.O. board are given in Table 7.

TABLE 7

B.F.O. Board: Signal Levels

Signal output		Control input		
Frequency	Pins	Level	Pin	Function
16.65 MHz	4 and 5	+11V	3	Osc. on
22 MHz	9 and 10	+11V	1	Osc. on
21.4 MHz ± 10 kHz	7 and 12	+11V	8	B.F.O. on
		+0.5V to +20V	11	B.F.O. tune

Note: The b.f.o.-on condition requires +11V on pins 1, 3 and 8.

25. The functions of all the semiconductor devices on the board are given in Table 8.

TABLE 8

B.F.O. Board: Semiconductor Functions

Semiconductor	Function
TR1, D2	Voltage-controlled oscillator, 22 MHz
TR2	Crystal oscillator, 16.65 MHz
IC1	Mixer
TR3, TR4	Frequency multiplier
TR5-7	Tuned amplifier, 21.4 MHz
TR8	Connects BFO TUNE potentiometer to 0V rail
D1	Zener diode

VIDEO AND AUDIO AMPLIFIER BOARD (fig. 13)

26. The purpose of the Video and Audio Amplifier board is to distribute the outputs from the F.M./C.W. Discriminator board. Five separate amplifier paths are provided; the input and output signal levels are given in Table 9. The audio outputs are fed to SKT3 and the video output to SKT6. The 15 mW output is also fed via the PHONES GAIN control to the PHONES jack on the receiver.

TABLE 9

Video and Audio Amplifier Board: Signal Levels

Input		Output		
Pins	Level	Function	Pins	Level
16 and T	15 mV r.m.s.	Video	13 and P	15 mW, 75 ohms
		Audio ('phones)	9 and K	15 mW, 100 ohms
1 and earth	200 mV r.m.s.	Audio, line	15 and S	1 mW, 600 ohms
		Audio, line	14 and R	1 mW, 600 ohms
		Loudspeaker	3 and C	50 mW, 25 ohms

27. The functions of all the semiconductor devices on the board are given in Table 10.

TABLE 10

Video and Audio Amplifier Board: Semiconductor Functions

Semiconductor	Function
IC1, IC2, TR1, TR2, D1, D2	Video amplifier
IC3, TR3, TR4, D3, D4	Audio amplifier, 15 mW
IC4 (part 1)	Audio amplifier, 1 mW
IC4 (part 2)	Audio amplifier, 1 mW
IC5, TR5, TR6, D5, D6	Loudspeaker amplifier

C.O.R./Serialiser/Squelch Board (fig. 15)

28. The C.O.R./Serialiser/Squelch board performs the following instructions:-

(1) Controls the action of the carrier-operated relay.

(2) Drives the SYN LOCK lamp.

(3) Generates the clock and serialiser data outputs.

(4) Generates the frame/load pulse for gating-in external equipment.

(5) Accepts serial data from the logic board and synchronises this data with the frame pulse.

(6) Provides audio-squelch facility.

29. The 5 kHz clock input (pin A) is processed to provide the output waveforms given in fig. 1. These outputs appear at pins 1, 2 and 9 of the board.

30. The AGC2 input (pin S) is compared with a reference voltage from the COR LEVEL potentiometer (pin R). When the AGC2 level is more positive than the reference voltage, the comparator output (IC7) is high and hence the relay and lamp are energized. Pin R has a range of -0.7V to +1.4V. The COR relay release-time is selected by the COR switch and is instantaneous or about 7 seconds; pin M is at +12V for the DELAY setting. The squelch relay RLA breaks the audio feed line when the comparator reference voltage is more positive than the AGC2 input. The operation of RLA is not delayed when the COR switch is in the DELAY position.

31. When the L.F., Transfer and H.F. loops of the synthesizer are all 'in-lock', 0V inputs are applied simultaneously to pins E, F and H of the control board; the resultant 0V output at pin D lights the SYN LOCK lamp.

32. The functions of all the semiconductor devices on the board are given in Table 11.

TABLE 11

C.O.R./Serialiser/Squelch Board: Semiconductor Functions

Semiconductor	Functions
TR2, TR4 and IC1 to IC5	Serialiser control
TR1, TR7, D1-3	Lock lamp driver
IC7	C.O.R. comparator
TR5	C.O.R. time-delay
TR6, IC6B, TR8	C.O.R. relay driver
IC6A	Squelch relay driver

CHAPTER 3

TECHNICAL DESCRIPTION

RECEIVER TUNING SYSTEM

INTRODUCTION

1. The receiver tuning system consists of the following sub-assemblies and printed-wiring boards; refer to fig. 37 for interconnections between the sub-assemblies.

   (1) Tuning encoder sub-assembly.

   (2) Logic board.

   (3) Intermediate logic board.

   (4) Frequency display sub-assembly including frequency display board and six l.e.d. assemblies.

TUNING ENCODER (fig. 16)

2. The tuning encoder is an optical displacement transducer of the incremental type. two circular graticules, one fixed and one rotatable, are situated in the light-path between two lamps and two phototransistors; the phototransistors are physically displaced such that a 90° phase difference exists between their outputs. Rotation of the 'tuning' control, and hence the moveable graticule, produces two sinusoidal output voltages of 4V-8V p-p* at pins 10 and 4. The potentiometers R1 and R2 set the output level from the phototransistor emitter-followers to a sinusoidal maximum.

LOGIC BOARD (fig. 18)

3. The function of all the semiconductor devices on the logic board is given in Table 1.

TABLE 1

Logic Board: Semiconductor Functions

Semiconductor	Function
IC44 and TR1	Squarer for 'A' tuning pulses
IC12 and TR2	Squarer for 'B' tuning pulses (up/down)
IC42, IC43, IC45, IC47-2, 3 and 4, IC46-1 and 3, IC20-3, IC48-1, IC49-3, IC50-1.	'A' tuning pulses rate control

* peak-to-peak

TABLE 1 (Cont'd)

Semiconductor	Function
IC48-2	Lock function (gate 1)
IC48-3, IC46-5	End-of-band function (gate 2)
IC1 to IC6, IC13	Synchronous/reversible counter (memory):- IC1, kHz x 1 IC2, kHz x 10 IC3, kHz x 100 IC4, MHz x 1 IC5, MHz x 10 IC6, MHz x 100
IC34 to IC37	Buffers
IC29, IC30, IC31-1 and 4, IC32, IC33	9's complement converter
IC38, IC39, IC40	Buffers
IC22, IC23	I.F. offset-adder
IC21, IC28, IC41	Serializer
IC10-1 to IC10-5, IC11, IC47-1, IC16-1, IC7, IC8, IC9, IC49-1 and 2, IC50-2 and 3, IC51-1, 2 and 3	Decoder and selector
IC14, IC18-2, IC15, IC19-1, IC16-2 to IC16-4, IC19-2, IC20-2, IC10-6, IC46-4 and 6, IC49-4, IC53, IC17-1 and IC17-2, IC18-1, IC20-1, IC48-4	Comparator

4. Rotation of the front-panel 'tuning' control produces a sinusoidal waveform of 4 to 8 volts p-p at pins W8 and W9 of the board; waveform A (pin W8) leads waveform B (pin W9) by 90° for clockwise rotation, and vice-versa for counter-clockwise rotation. With either the FAST or SLOW pushbuttons depressed the frequency display changes in 100 kHz or 1 kHz increments respectively. The levels at pin W7 of the board are either +5V or 0V (nom.) for the 'fast' or 'slow' tuning conditions respectively.

5. When the LOCK pushbutton is depressed, the level at pin W6 of the board is +5V; when 'fast' or 'slow' tuning, this level drops to 0V.

6. The range-code levels at pins ZL, Z10, ZP, ZR, Z1 and Z6 are summarised in Table 2 for each range of the three R.F. Tuner Heads.

TABLE 2

Range Code Levels

Range	Range Code Level					
	Pin ZL	Pin Z10	Pin ZP	Pin ZR	Pin Z1	Pin Z6
20 - 40 MHz	0V	+5V	+5V	+5V	+5V	+5V
40 - 90 MHz	+5V	0V	+5V	+5V	+5V	+5V
90 - 195 MHz	+5V	+5V	0V	+5V	+5V	+5V
195 - 400 MHz	+5V	+5V	+5V	0V	+5V	+5V
400 - 650 MHz	+5V	+5V	+5V	+5V	0V	+5V
650 - 1000 MHz	+5V	+5V	+5V	+5V	+5V	0V

7. At the instant of switching on the receiver, with the LOCK pushbutton depressed, the levels on the output pins to the frequency readout unit are as shown in Table 3 (levels A); depressing the LOCK pushbutton ensures that, when making measurements, accidental movement of the 'tuning' control has no effect on the switch-on state of the 'memory' Note that Table 3 is in normal BCD form, and that the output levels are preset to one end of the selected frequency band or range.

8. The presence of these levels is a strong indication that the logic board is functioning correctly. Assuming that no faults exist in the frequency readout unit, the preset frequency will be displayed in accordance with the selected frequency range.

TABLE 3

Output Levels to Frequency Readout Units

R.F. Tuner	20 - 90 MHz				90 - 400 MHz				400 - 1000 MHz			
Range	20 -40 MHz		40-90 MHz		90-195 MHz		195-400 MHz		400-650 MHz		650-1000 MHz	
Board Pin	Level		Level		Level		Level		Level		Level	
	A	B	A	B	A	B	A	B	A	B	A	B
ZA	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V
Z2	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V
Z3	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V
Z4	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V
Z5	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V
Z7	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V
Z8	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V
Z9	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V
ZS	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	+5V
Z11	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V
Z12	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	0V
Z13	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	+5V
Z14	0V	+5V	+5V	0V	+5V	+5V	0V	0V	0V	+5V	+5V	+5V
Z15	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V
Z16	0V	0V	0V	0V	+5V	0V	+5V	0V	0V	0V	0V	0V
ZB	0V	+5V	+5V	0V	0V	+5V	0V	0V	0V	+5V	+5V	+5V
ZC	0V	+5V	+5V	+5V	+5V	0V	+5V	0V	+5V	+5V	0V	+5V
ZD	0V	0V	+5V	0V	0V	0V	0V	0V	0V	0V	0V	0V
ZE	+5V	0V	0V	0V	0V	0V	0V	0V	+5V	0V	+5V	0V
ZH	0V	0V	0V	+5V	+5V	+5V	+5V	0V	0V	+5V	0V	+5V

TABLE 3 (Cont'd)

R.F. Tuner	20 - 90 MHz				90 - 400 MHz				400 - 1000 MHz			
Range	20-40 MHz		40-90 MHz		90-195 MHz		195-400 MHz		400-650 MHz		650-1000 MHz	
Board Pin	Level		Level		Level		Level		Level		Level	
	A	B	A	B	A	B	A	B	A	B	A	B
ZJ	0V	0V	0V	0V	+5V	0V	+5V	0V	0V	+5V	0V	+5V
ZK	0V	0V	0V	0V	0V	0V	0V	0V	+5V	+5V	+5V	0V
ZT	0V	0V	0V	0V	0V	0V	0V	+5V	+5V	0V	+5V	0V
ZM	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	+5V

Note: 'A' denotes levels at the preset (switch-on) frequencies:-
40.499, 39.499, 195.499, 194.499 MHz, 650.499 MHz, 649.499 MHz.

'B' denotes levels at the end-of-band frequencies:-
19.499, 90.499, 89.499, 400.499 MHz, 399.499 MHz, 999.999 MHz.

9. If the SLOW pushbutton is depressed and the 'tuning' control is slowly rotated in the appropriate direction for the band selected, the display changes in increments of 1 kHz; when the FAST pushbutton is depressed, the display changes in100 kHz increments.

10. The display will change in sympathy with the 'tuning' control until the end-of-band frequency is reached. At this point, the changes in output level - and hence the display - are halted.

11. If the tuning is continued past this point, the display remains at the end-of-band value; the output levels for this condition are given in Table 3 (levels B).

12. Assuming that no faults exist in the frequency readout unit, and that the display is not yielding the expected result, then a fault will exist on the logic board or in the interconnections.

13. With the conditions in para. 7 prevailing, the levels on the output pins to the synthesizer are as shown in Table 4, which is produced from a 9's complement BCD truth table; these BCD levels include tha appropriate 1st i.f., less an additional 2 MHz inherent in the synthesis process (Chap. 4, para. 10), viz. 120 or 70 (90-195 MHz range only). It is assumed that no faults exist in the output buffer stages (Table 1) to the synthesizer.

14. The output from the serialiser is applied to external equipment, and an incorrect response from this equipment, when the conditions of para. 1 and Table 3 prevail, could be attributed to a fault on the logic board. The amplitude and frequency of the serialiser clock input at pin W13 are 5V p-p at 5 kHz (internal). Fig. 1 is a timing diagram for the load/shift control (pin 11) and data output (pin 12), as related to the serialiser clock pulses (pin 13). The facility exists for operating the serialiser from an external clock source in the range 1 kHz to 25 kHz.

TABLE 4

Output Levels to Synthesizer

R.F. Tuner	20-90 MHz				90-400 MHz				400-1000 MHz			
Range	20-40 MHz		40-90 MHz		90-195 MHz		195-400 MHz		400-650 MHz		650-1000 MHz	
Board Pin	Level		Level		Level		Level		Level		Level	
	A	B	A	B	A	B	A	B	A	B	A	B
X7	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V
X8	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V
X9	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V
X10	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V
X1	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V
X2	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V
X5	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V
X4	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V
X3	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	0V
X6	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V
X14	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	0V
X15	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V
Y1	+5V	0V	0V	+5V	0V	0V	+5V	+5V	+5V	0V	0V	0V
Y4	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V
Y3	0V	0V	0V	0V	+5V	0V	+5V	0V	0V	0V	0V	0V
Y2	+5V	0V	0V	+5V	0V	0V	0V	+5V	+5V	0V	0V	0V

TABLE 4 (Cont'd)

R.F. Tuner	20-90 MHz				90-400 MHz				400-1000 MHz			
Range	20-40 MHz		40-90 MHz		90-195 MHz		195-400 MHz		400-650 MHz		650-1000 MHz	
Board Pin	Level A	B	Level A	B	Level A	B	Level A	B	Level A	B	Level A	B
Y6	+5V	0V	0V	0V	+5V	0V	0V	+5V	0V	0V	+5V	0V
Y10	+5V	+5V	0V	0V	+5V	0V	0V	+5V	+5V	0V	+5V	0V
Y13	0V	+5V	+5V	0V	0V	+5V	0V	+5V	0V	0V	0V	0V
Y11	0V	0V	0V	+5V	0V	0V	+5V	0V	0V	+5V	0V	+5V
Y8	0V	0V	0V	+5V	+5V	0V	0V	0V	0V	0V	0V	0V
Y7	0V	0V	0V	+5V	+5V	0V	+5V	0V	+5V	0V	+5V	0V
Y5	0V	0V	0V	+5V	+5V	0V	+5V	+5V	0V	+5V	0V	0V
Y9	+5V	+5V	+5V	0V	0V	+5V	0V	0V	0V	0V	0V	+5V

Notes: 'A' denotes levels at the preset (switch-on) frequencies:- 40.499, 39.499, 195.499, 194.499 MHz, 650.499 MHz, 649.499 MHz.

'B' denotes levels at the end-of-band frequencies:- 19.499, 90.499, 89.499, 400.499 MHz, 399.499 MHz, 999.999 MHz.

15. The low-level supply voltages to the board are shown on the circuit diagram (fig. 18) against the relevant pins on the board.

BATTERY STANDBY BOARD (fig. 20)

16. The power for the logic board is fed via the battery board so that, in the event of a mains failure of up to three hours duration, the logic levels for the receiver frequency setting will be maintained.

17. The battery standby supply comprises three series-connected 1.2V nickel-cadmium cells, each of 50 mAh capacity. The cells are trickle-charged from the +12V rail when the POWER switch is set to ON; the charge and discharge rates are about 1 mA. With the POWER switch set to OFF, there is no connection to the nickel-cadmium batteries.

18. Table 5 gives the voltage levels at the board pins for STBY (standby) and ON positions of the POWER switch. Should D2 fail, it is important that the replacement diode should be of the same type.

TABLE 5

Battery Standby Board: Voltage Levels

	POWER switch	
Pin	STBY	ON
L	0V	0V
E	+3.6V	+3.6V
D	+3.6V	+3.6V
B	0V	+12V
F	0V	+5V
A	+3.4V	+4.3V

INTERMEDIATE LOGIC BOARD (fig. 22)

19. The purpose of the intermediate logic board is to distribute the BCD output lines from the memory to the three synthesizer loops. The H.F. and Transfer loops are programmed by the X4, X5 and X6 decades in the memory; the L.F. loop is programmed by the X1, X2 and X3 decades. For the conditions prevailing in para. 7, the levels on the output pins of the board can be derived from Table 4.

FREQUENCY DISPLAY UNIT (fig. 24)

20. The BCD lines from the logic board (Table 3) are applied to the frequency display unit which contains six BCD/7-segment decoding and driver stages for the l.e.d. display units. With the conditions in para. 7 prevailing, then if the display is incorrect when the levels at the input pins are in accordance with Table 3, a fault exists on the board.

CHAPTER 4

TECHNICAL DESCRIPTION

RECEIVER SYNTHESIZER AND 2ND LOCAL OSCILLATOR

INTRODUCTION

1. The receiver synthesizer consists of the 5 MHz frequency standard and the following printed-wiring boards; refer to fig. 37 for board interconnections.

   (1) Divider board.

   (2) L.F. Loop board.

   (3) Transfer Loop board.

   (4) H.F. Loop board.

   (5) Interconnection board.

This chapter also describes the 2nd Local Oscillator board. Descriptive and maintenance information for the 5 MHz frequency standard are not given in this handbook because this assembly can only be serviced by the manufacturer; however, measurement of the first level in Table 4 confirms that it is functioning correctly. The numerical examples of the three v.c.o. frequencies given during the following paragraphs relate to a displayed frequency of 40.499 MHz.

DIVIDER BOARD (fig. 26)

2. The functions of the divider board are as follows:-

   (1) to distribute 5 MHz to the transfer loop and the 2nd local oscillator,

   (2) to produce 5 kHz for the L.F. loop and the serializer control stage.

3. The signal levels at the pins on the board are given in Table 1.

TABLE 1

Divider Board : Signal Levels

Signal	Pin No.	Level
5 MHz input	1 and 2 (0V)	100-250 mV p-p
5 MHz output	3 and 4 (0V)	TTL
5 kHz output	9 and 8 (0V)	TTL
5 kHz output	7 and 6 (0V)	TTL
1 MHz test	15 and 5 (0V)	TTL
500 kHz test	14 and 5 (0V)	TTL
100 kHz test	13 and 5 (0V)	TTL
50 kHz test	12 and 5 (0V)	TTL
10 kHz test	11 and 5 (0V)	TTL

L.F. LOOP BOARD (fig. 28)

4. The function of all semiconductor devices on the board is given in Table 2.

TABLE 2

L.F. Loop Board : Semiconductor Functions

Semiconductor	Function
IC2, IC3, IC4, IC5, IC6 TR3, TR4	Synchronous divider N2
D2, IC1	Voltage controlled oscillator
TR2, TR1	Loop output stage
IC7, IC8-1	Phase-comparator
TR7, TR6, TR5	Digital-analogue converter
IC8-3, 4 and 5	In-Lock signal stage

5. The 9's complemented BCD levels which programme the synchronous divider N2 are produced by the X1, X2 and X3 counters in the logic memory; Table 4 of Chapter 3 gives the preset logic levels, produced at the output pins of the Logic board, for the receiver frequency setting at the instant of switching on (preset frequency) and at the end of each band. Table 3 of this chapter repeats these levels as related to the pins on the L.F. Loop board; it should be noted that the levels on the X3, X2 and X1 lines represent the 'kHz' part of the synthesizer frequency.

TABLE 3

Input Levels to Programmed Divider N2 (L.F. Loop)

R.F. Tuner		20 - 90 MHz				90 -400 MHz				400 - 1000 MHz			
Range		20-40 MHz		40-90 MHz		90-195 MHz		195-400 MHz		400-650 MHz		650-1000 MHz	
Board Pin		Level A	B	Level A	B	Level A	B	Level A	B	Level A	B	Level A	B
13	X1	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V
14		0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V
15		0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V
12		0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V
7	X2	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V
8		0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V
9		0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V
6		0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V
2	X3	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	0V
3		0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V
4		+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	0V
1		0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V

Note: 'A' denotes levels at the preset (switch-on) frequencies:-
40.499, 39.499, 195.499, 194.499 MHz, 650.499 MHz, 649.499 MHz.

'B' denotes levels at the end-of-band frequencies:-
19.499, 90.499, 89.499, 400.499, 399.499, 999.999 MHz

6. The signal levels which normally exist at the remaining pins on the board, for the conditions stated in para. 5, are given in Table 4. D.C. supply levels are shown on fig. 28.

7. The frequency of the voltage-controlled oscillator (12.495 MHz at pin 20) is derived in the following manner. The X3, X2 and X1 input levels (Table 3, 40.499 MHz) are the 9's complemented BCD levels for the digits 4, 9 and 9 respec.tively; the oscillator frequency is expressed as:-

(2000 + N2) 5 kHz

viz. (2000 + 499) 5 kHz = 12.495 MHz

For any other frequency setting, the BCD levels on the X3, X2 and X1 lines can be measured and converted to decimal form using Table 5; the oscillator frequency can then be calculated as above. Note that pins 13, 7 and 2 (Table 3) are the 2^0 binary digits and that X1 is the least significant number.

TABLE 4

L.F. Loop Board : Signal Levels

Pins	20, 21 (0V)	16, 17 (0V)	18, 17 (0V)
Level	TTL 12.495 MHz	TTL 5 kHz	+5V (nom.): out-of-lock. 0V: in-lock.

TABLE 5

9's Complemented BCD Levels

	2^3	2^2	2^1	2^0
0	+5V	0V	0V	+5V
1	+5V	0V	0V	0V
2	0V	+5V	+5V	+5V
3	0V	+5V	+5V	0V
4	0V	+5V	0V	+5V
5	0V	+5V	0V	0V
6	0V	0V	+5V	+5V

TABLE 5 (Cont'd)

	2^3	2^2	2^1	2^0
7	0V	0V	+5V	0V
8	0V	0V	0V	+5V
9	0V	0V	0V	0V

8. If the L.F. Loop fails to lock, the level at pin 18 falls to a nominal +5V and the expected frequency at pin 20 will be abnormal.

TRANSFER LOOP BOARD (fig. 30)

9. The function of all semiconductor devices on the board is given in Table 6.

TABLE 6

Transfer Loop Board : Semiconductor Functions

Semiconductor	Function
IC3, IC4, IC5, IC6, IC7	Synchronous divider N1
D2, IC1	Voltage-controlled oscillator
TR2, TR3	Loop output stage
TR4	Amplifier buffer
IC2	Mixer
TR5	Amplifier buffer
IC8, IC9-1	Phase comparator
TR11, TR10, TR9	Digital-analogue converter
TR6, TR7, TR8	D.C. regulator
IC9-3, 4 and 5	In-lock signal stage

10. The 9's complemented BCD levels which programme the synchronous divider N1 are produced by the X4, X5 and X6 counters in the logic memory; Table 4 (Chap. 3) gives the logic levels, produced at the output pins of the Logic board, for the receiver frequency setting at the instant of switching on (preset frequency) and at the end

of each band. Table 7 of this chapter repeats these levels as related to the pins on the Transfer Loop board; it should be noted that the levels on the X6, X5 and X4 lines represent the 'MHz' part of the synthesizer frequency together with the 1st i.f. (122 MHz or 72 MHz) less 2 MHz viz 40 + (122-2) = 160 MHz.

TABLE 7

Input Levels to Programmed Divider N1 (Transfer Loop)

R.F. Tuner		20 - 90 MHz				90 - 400 MHz				400 - 1000 MHz			
Range		20-40 MHz		40-90 MHz		90-195 MHz		195-400 MHz		400-650 MHz		650-1000 MHz	
Board Pin		Level A	B	Level A	B	Level A	B	Level A	B	Level A	B	Level A	B
4	X4	+5V	0V	0V	+5V	0V	0V	+5V	+5V	+5V	0V	0V	0V
1		0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V
2		0V	0V	0V	0V	+5V	0V	+5V	0V	0V	0V	0V	0V
3		+5V	0V	0V	+5V	0V	0V	0V	+5V	+5V	0V	0V	0V
10	X5	+5V	0V	0V	0V	+5V	0V	0V	+5V	0V	0V	+5V	0V
7		+5V	+5V	0V	0V	+5V	0V	0V	+5V	+5V	0V	+5V	0V
8		0V	+5V	+5V	0V	0V	+5V	0V	+5V	0V	0V	0V	0V
9		0V	0V	0V	+5V	0V	0V	+5V	0V	0V	+5V	0V	+5V
14	X6	0V	0V	0V	+5V	+5V	0V	0V	0V	0V	0V	0V	0V
11		0V	0V	0V	+5V	+5V	0V	+5V	0V	+5V	0V	+5V	0V
12		0V	0V	0V	+5V	+5V	0V	+5V	+5V	0V	+5V	0V	0V
13		+5V	+5V	+5V	0V	0V	+5V	0V	0V	0V	0V	0V	+5V

Note: 'A' denotes levels at the preset (switch-on) frequencies:-
40.499, 39.499, 195.499, or 194.499, 650.499, 649.499 MHz

'B' denotes levels at the end-of-band frequencies:-
19.49, 90,499, 89.499, 400.499, 399.499, 999.999 MHz

11. The signal levels which normally exist at the remaining pins on the board for the conditions stated in para. 10, are given in Table 8. D.C. supply levels are shown in fig. 30.

TABLE 8

Transfer Loop Board : Signal Levels

Pins	25, 20 (0V)	21, 20 (0V)	15, 20 (0V)	24, 20 (0V)
Level	TTL 12.495 MHz	TTL 5.078 MHz	TTL	+5V (nom.): out-of-lock. 0V: in-lock.

12. The frequency of the voltage-controlled oscillator (5.078 MHz at pin 21) is derived in the following manner. The X6, X5 and X4 input levels (Table 7 40.499 MHz) are the 9's complemented BCD levels for the digits 1, 6 and 0 respectively; the number 160 is the division ratio to which the programmed divider is set. The oscillator frequency is expressed as:-

$$\frac{(2000 + N2)5}{N1} \text{ kHz} + 5 \text{ MHz}$$

viz $\frac{12.495}{160}$ MHz + 5 MHz = 5.078 MHz

For any other frequency setting, the BCD levels on the X6, X5 and X4 lines can be measured and converted to decimal form using Table 5; the oscillator frequency can then be calculated as above. Note that pins 4, 10 and 14 are the 2^0 binary digits and that X4 is the least significant number.

13. If the loop fails to lock, the level at pin 24 falls to a nominal +5V and the expected frequency at pin 21 will be abnormal.

H.F. LOOP BOARD (fig. 32)

14. As previously stated, the voltage-controlled oscillator for the H.F. Loop is the receiver 1st local oscillator and is contained in the R.F. Tuner Head (Part 3). Hence, the H.F. Loop board contains, in addition to two fixed dividers, only the phase-comparator and the programmed divider N1. The function of all semiconductor devices on the board is given in Table 9.

TABLE 9

H.F. Loop Board : Semiconductor Functions

Semiconductor	Function
IC2, IC3, IC4, IC5, IC6 IC1, TR1	Programmed divider N1
IC11, IC12-1	Phase comparator
TR2, TR3, TR4	Digital-analogue converter
IC8	
IC9	Divide-by-five
IC10	Divide-by-N3
IC12-2, 3 and 4	In-lock signal stage

15. The 9's complemented BCD levels which programme the synchronous divider N1 are produced by the X4, X5 and X6 counters in the logic memory and, hence, are the same as for the Transfer Loop. Table 4 (Chap. 3) gives the logic levels, produced at the output pins of the Logic board, for the receiver frequency setting at the instant of switching on (preset frequency) and at the end of each band. Table 10 of this chapter repeats these levels, which are the same as in Table 7 related to the pins on the H.F. Loop board; again, as stated in para. 10, the X6, X5 and X4 levels represent 160 MHz i.e. 40 + (122-2).

16. The frequency range of the H.F. Loop depends upon the R.F. range selected. This is achieved by range code levels, applied at pins 18 to 21, which preset the division ratio (via IC8) of divider N3. Table 11 summarises the range code levels and the resultant N3 division factor. A second preset divider N4, within the H.F. Loop is contained in the R.F. Tuner Head (Part 3). The N4 division factor is also given in Table 11.

17. The signal levels which normally exist at the remaining pins on the board, for the conditions stated in para. 15, are given in Table 12. D.C. supply levels are shown on fig. 32.

TABLE 10

Input Levels to Programmed Divider N1 (H.F. Loop)

R.F. Tuner		20 - 90 MHz				90 - 400 MHz				400 - 1000 MHz			
Range		20-40 MHz		40-90 MHz		90-195 MHz		195-400 MHz		400-650 MHz		650-1000 MHz	
Board Pin		Level A	B	Level A	B	Level A	B	Level A	B	Level A	B	Level A	B
15	X4	+5V	0V	0V	+5V	0V	0V	+5V	+5V	+5V	0V	0V	0V
14	X4	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V
13	X4	0V	0V	0V	0V	+5V	0V	+5V	0V	0V	0V	0V	0V
12	X4	+5V	0V	0V	+5V	0V	0V	0V	+5V	+5V	0V	0V	0V
11	X5	+5V	0V	0V	0V	+5V	0V	0V	+5V	0V	0V	+5V	0V
10	X5	+5V	+5V	0V	0V	+5V	0V	0V	+5V	+5V	0V	+5V	0V
9	X5	0V	+5V	+5V	0V	0V	+5V	0V	+5V	0V	0V	0V	0V
8	X5	0V	0V	0V	+5V	0V	0V	+5V	0V	0V	+5V	0V	+5V
7	X6	0V	0V	0V	+5V	+5V	0V	0V	0V	0V	0V	0V	0V
6	X6	0V	0V	0V	+5V	+5V	0V	+5V	0V	+5V	0V	+5V	0V
5	X6	0V	0V	0V	+5V	+5V	0V	+5V	+5V	0V	+5V	0V	0V
4	X6	+5V	+5V	+5V	0V	0V	+5V	0V	0V	0V	0V	0V	+5V

Note: 'A' denotes levels at the preset (switch-on) frequencies:-
40.499, 39.499, 195.499, 194.499, 650.499, 649.499 MHz.

'B' denotes levels at the end-of-band frequencies:-
19.499, 90.499, 89.499, 400.499, 399.499, 999.999 MHz.

TABLE 11

Range Code Levels and N3/N4 Division Factors (H.F. Loop)

R.F. Head Range (MHz)	Range Code Levels				Division Factor	
	Pin 19	Pin 20	Pin 21	Pin 18	N3	N4
20-40 and)	0V	+5V	0V	0V	1	1
40-90)	0V	+5V	0V	0V	2	2
90-195 and)	0V	0V	+5V	0V	2	2
195-400)	0V	0V	+5V	0V	4	4
400-650 and)	0V	0V	+5V	0V	4	4
650-1000)	0V	0V	0V	+5V	8	4

TABLE 12

H.F. Loop Board : Signal Levels

Pins	23, 22 (0V)	17, 16 (0V)	26, 25 (0V)	1, 16 (0V)	29, 27 (0V)
Level	TTL 5.078 MHz	800 ± 200 mV p-p 162.499 MHz	3V (l.f.) to 9V (h.f.)	+5V d.c.	+5V (nom.): out-of-lock 0V: in-lock.

18. The frequency of the voltage-controlled oscillator (162.499 MHz at pin 17) is derived in the following manner. The X6, X5 and X4 input levels (Table 10, 40.499 MHz) are the 9's complemented BCD levels for the digits 1, 6 and 0 respectively (para. 12); the number 160 is the division ratio to which the programmed divider is set. The oscillator frequency is expressed as:-

$$\left[\frac{(2000 + N2)5}{N1}\ \text{kHz} + 5\ \text{MHz}\right] \times \frac{N1 . N4}{5 . N3}$$

which simplifies to:-

$$\left[\frac{(2000 + N2}{N1}\ \text{kHz} + 1\ \text{MHz}\right] \times \frac{N1 . N4}{N3}$$

From Table 11, it will be seen that:-

$$N3 = N4$$

Hence the above expression further simplifies to:-

N2 kHz + N1 MHz + 2 MHz

Therefore, the frequency of the voltage-controlled oscillator, for the conditions stated in para. 15, is as follows:-

499 kHz + 160 MHz + 2 MHz

viz. 162.499 MHz

19. For any other frequency setting, the BCD levels on the X6, X5, X4, X3, X2 and X1 can be measured and converted to decimal form using Table 5; the X3, X2 and X1 levels provide the N2 factor and the X6, X5 and X4 levels provide the N1 factor. The oscillator frequency can then be calculated as above.

20. If the loop fails to lock, the level at pin 29 falls to a nominal +5V and the expected frequency at pin 17 will be abnormal.

2nd LOCAL OSCILLATOR

21. The 2nd Local Oscillator generates either of two frequencies depending upon the receiver range selected; the voltage-controlled oscillator forms part of a phase-lock loop and Table 13 summarises all the main signal frequencies including that of the 2nd local oscillator.

TABLE 13

Receiver Signal Frequencies (MHz)

Band	1st V.C.O.	1st I.F.	2nd V.C.O.	2nd I.F.
19.499 - 40.499	141.499 - 162.499	122	143.4	21.4
39.499 - 90.499	161.499 - 212.499	122	143.4	21.4
89.499 - 195.499	161.499 - 267.499	72	93.4	21.4
194.499 - 400.499	316.499 - 522.499	122	143.4	21.4
399.499 - 650.499	521.499 - 722.499	122	143.4	21.4
649.499 - 999.999	771.499 - 1121.499	122	143.4	21.4

22. The function of all semiconductor devices on the board is given in Table 14.

TABLE 14

2nd Local Oscillator : Semiconductor Functions

Semiconductor	Function
D2, D3, D4, D5, TR1	Voltage-controlled oscillator
TR2	Amplifier
TR3	Loop output stage
TR4, TR5	Amplifier
IC1	Mixer
IC2, TR6a and b	Phase comparator
TR7, TR8	1.6 MHz crystal-controlled oscillator

23. The signal levels which exist at the pins on the board are given in Table 15. D.C. supply levels are shown on fig. 34.

TABLE 15

2nd Local Oscillator : Signal Levels

		Range			
		20 - 90 MHz 195 - 1000 MHz		90 - 195 MHz	
Pins	11, 10 (0V)	4, 10 (0V)	6, 5 (0V)	4, 10 (0V)	6, 5 (0V)
Level	TTL	Open-circuit	600 mV r.m.s. 143.4 MHz	+5V d.c.	600 mV r.m.s 93.4 MHz

CHAPTER 5

FAULT FINDING

INTRODUCTION

1. This chapter gives a guide to fault-finding to printed-wiring board level. A symptom may become apparent from headphone monitoring, from observance of the function-indicators, frequency display and tuning meter on the receiver unit. A symptom such as reduced or zero video/audio output may also become apparent from the behaviour of external equipment. The fault is localised by manipulation of the front panel controls together with level measurements.

2. If a complete set of boards is available as serviceable spares, the board substitution method is recommended. Where the boards are not of the plug-in variety, use of the following guide will avoid the unnecessary removal of wired-in sub-assemblies.

3. The following routine is recommended, and is detailed in the succeeding paragraphs.

(1) Check the power supply voltages (Chap. 1, para. 3).

(2) Check the frequency display system (para. 8).

(3) Check the tuning system (para. 10).

(4) Check the synthesizer loop oscillators (para. 13).

(5) Check the 2nd local oscillator (para. 16).

(6) Check the r.f. tuner head (Part 3, 4 or 5, as appropriate).

(7) Check the i.f. processing stages (para. 19).

(8) Check the auxiliary outputs (para. 29).

(9) Check the signal display system (Part 2, if relevant).

4. This entire chapter should first be read, because the proposed routines establish suitable methods for fault symptoms other than abnormal output from the receiver. Since the signal levels are detailed in the technical description chapters, cross-references are made to these chapters as necessary.

5. The procedures assume that a fault symptom such as zero audio output has been noted and that the receiver has been switched off prior to fault-finding. It is also assumed that all fuses and lamps have been checked and found to be serviceable (Chap. 4, Operator's Handbook), and that the frequency standard is functioning correctly

(refer to para. 1 of Chap. 4).

TEST EQUIPMENT

6. The following items of test equipment are required (refer to Chap.7, Table 1):

(1) Multimeter (AVO 9SX).

(2) Electronic voltmeter and probe.

(3) Frequency counter and probe.

(4) Oscilloscope.

(5) Signal generator.

7. The electronic voltmeter and probe (item 2) are used for all r.f. level measurements. When making frequency measurements, use the high-impedance probe with the frequency counter (item 3). Logic levels may be checked with the multimeter (item 1).

FREQUENCY DISPLAY CHECK

8. (1) Assuming the 20-90 MHz R.F. Tuner Head is installed, select the 20-40 MHz range.

(2) Switch on the receiver and depress the LOCK pushbutton.

(3) Check the range code levels in accordance with Table 2 (Chap. 3).

(4) Check that the frequency displayed (preset) is in accordance with Table 1.

(5) Depress the FAST pushbutton and tune the receiver to the end-of-band frequency; check that the frequency is as given in Table 1.

(6) Select the 40-90 MHz range and repeat operations (3) to (5).

(7) As appropriate, repeat the above procedure using the 90-400 MHz and 600-1000 MHz Head Tuner.

9. If the results obtained do not agree with Table 1, measure the logic levels shown in Table 3 (Chap. 3). If these levels are correct, the Frequency Display assembly is faulty; alternatively, the Logic board is faulty.

TABLE 1

Preset and End-of-Band Frequencies

Band	Range	Preset Frequency	End-of-Band Frequency
1	20 - 40 MHz	40.499 MHz	19.499 MHz
2	40 - 90 MHz	39.499 MHz	90.499 MHz
3	90 - 195 MHz	195.499 MHz	89.499 MHz
4	195 - 400 MHz	194.499 MHz	400.499 MHz
5	400 - 650 MHz	650.499 MHz	399.499 MHz
6	650 - 1000 MHz	649.499 MHz	999.999 MHz

TUNING SYSTEM

10. Assuming the frequency display system is functioning correctly and that the expected preset and end-of-band displays are obtained, check that the logic levels are in accordance with Table 4 (Chap. 3) for the previous conditions. If the levels are incorrect, the Logic board is faulty.

11. The correct functioning of the 'fast' and 'slow' tuning facility can be checked at this stage. Depress, in turn, the FAST and SLOW pushbuttons and observe in each instance that 'spinning' the Tuning control causes the display to change in 100 kHz and 1 kHz increments respectively. If not, either the Tuning Encoder Assembly or the Logic board may be faulty.

12. If the fault symptom is an abnormal serial-data output, use the oscilloscope to check the data levels as shown in fig. 1. Either the Logic board or the COR/Serialiser board may be at fault.

SYNTHESIZER

13. Check the Divider board by carrying out the measurements contained in Table 1 of Chap. 4. The assumption is now made that the Tuning Encoder, Logic board, Frequency Display board and Divider board are functioning correctly. Hence, assuming no faults exist on the Intermediate Logic board, then the logic levels shown in Tables 3, 7 and 10 of Chap. 4 are correct for the preset and end-of-band conditions.

14. Should it be required to ascertain the logic levels into the synthesizer for any frequency within a band, proceed as follows:-

(1) Assume a displayed frequency of 28.375 MHz in band 1, viz:-

028 MHz
+
375 kHz

(2) Add 120 MHz (i.e. 122 less 2 MHz for bands 1, 2, 4, 5 and 6) or 70 MHz (i.e. 72 less 2 MHz for band 3).

(3) Refer to Table 5 of Chap. 4 (9's complemented BCD levels) in order to obtain the levels given in the following Table 2.

TABLE 2

Synthesizer Input Levels for an Arbitrary Frequency

Freq. MHz	L.F. Loop (N2)		Transfer loop (N1)		H. F. Loop (N1)		
	Pin	Level	Pin	Level	Pin	Level	
0.005	13	0V	-	-	-	-	2^0
	14	0V	-	-	-	-	2^1
	15	+5V	-	-	-	-	2^2
	12	0V	-	-	-	-	2^3
0.07	7	0V	-	-	-	-	2^0
	8	+5V	-	-	-	-	2^1
	9	0V	-	-	-	-	2^2
	6	0V	-	-	-	-	2^3
0.3	2	0V	-	-	-	-	2^0
	3	+5V	-	-	-	-	2^1
	4	+5V	-	-	-	-	2^2
	1	0V	-	-	-	-	2^3
8	-	-	4	+5V	15	+5V	2^0
	-	-	1	0V	14	0V	2^1
	-	-	2	0V	13	0V	2^2
	-	-	3	0V	12	0V	2^3

TABLE 2 (Cont'd)

Freq. MHz	L.F. Loop (N2)		Transfer Loop (N1)		H.F. Loop (N1)		
	Pin	Level	Pin	Level	Pin	Level	
4	-	-	10	+5V	11	+5V	2^0
	-	-	7	0V	10	0V	2^1
	-	-	8	+5V	9	+5V	2^2
	-	-	9	0V	8	0V	2^3
1	-	-	14	0V	7	0V	2^0
	-	-	11	0V	6	0V	2^1
	-	-	12	0V	5	0V	2^2
	-	-	13	+5V	4	+5V	2^3

Note: Synthesizer setting of 148.375 MHz corresponds to a 28.375 MHz display frequency.

IMPORTANT NOTE

Under fault conditions, the presence of a supposedly correct frequency display does not imply that the synthesizer has tuned the receiver to the displayed frequency.

15. When glowing, the SYN LOCK lamp indicates that the three synthesizer loop oscillators are phase 'locked'. In order to confirm that these oscillators are generating the correct frequencies proceed as follows:-

(1) Check the range code levels as given in Table 11 (Chap. 4).

(2) Using the electronic voltmeter, check all loop signal levels as given in Tables 4, 8 and 12 (Chap. 4).

(3) Using a suitable frequency counter, check the operating frequency of each loop oscillator; these operating frequencies are calculated in the manner shown in para. 7 (L.F. Loop), 12 (Transfer Loop) and 18 (H.F. Loop) of Chap. 4. Note that the H.F. Loop oscillator is, in effect, the first local oscillator.

2nd LOCAL OSCILLATOR

16. The 2nd local oscillator is checked by carrying out the measurements given in Table 15 of Chap. 4.

R.F. TUNER HEADS

17. Under normal conditions, the r.f. signal at the antenna results in a 1st i.f. output from the r.f. Tuner Head (72 MHz or 122 MHz signals according to the band selected) and a corresponding 2nd i.f. output (21.4 MHz). The presence of the 2nd i.f. output (IF No. 1 at SKT5) is therefore a good indication that the tuner heads are functioning correctly; a faulty head will be self-evident by substitution.

18. Refer to Part 3, 4 or 5 of this handbook which give full servicing information for the R.F. Tuner Heads.

I.F. PROCESSING

19. The presence-or otherwise of the 1st i.f. output localises a signal fault to the '2nd mixer onwards' part of the receiver. The existance of this signal will now be assumed.

20. A symptom of reduced or zero video and audio output from the receiver indicates a fault in the 'common' signal path:-

(1) 2nd Mixer and Filter board.

(2) I.F. Amplifier board.

(3) F.M./C.W. Detector board.

(4) Video and Audio Amplifier board.

The signal levels and control potentials for these boards and for the B.F.O. board are given in Chap. 2.

21. A reduced or zero output (21.4 MHz at SKT5) from the 2nd mixer indicates a fault in the 2nd Mixer and Filter board - the selection prior to test point TP1.

22. Assuming the output at SKT5 is correct, measure the i.f. output levels from the 2nd Mixer and Filter board (terminals 19 and 20) to the I.F. Amplifier board; select each mode and i.f. bandwidth in turn. If an unsatisfactory output is obtained for one or more settings of the IF BANDWIDTH kHz switch - with appropriate MODE switch settings - measure the control potentials as given in Table 3 of Chap. 2; if these levels are correct, the fault is in the relevant section of the 2nd Mixer and Filter board. If no output is obtained for any IF BANDWIDTH kHz setting, the i.f. output stage may be faulty.

23. Measure the 21.4 MHz signal outputs from the I.F. Amplifier board:-

(1) via terminals 7 and 8 to the F.M./C.W. Detector board.

(2) via terminals 9 and 10 to the F.M./C.W. Detector board.

(3) via terminals 5 and 6 to SKT4.

Each of these outputs should be present at all settings of the MODE switch.

24. The 2nd Mixer and Filter board and the I.F. Amplifier board should now be functioning correctly with respect to the 21.4 MHz paths. Select the AM mode and the IF BANDWIDTH - 6 kHz setting and, using an appropriate test signal, measure the video and audio outputs. If all the audio and the video outputs are incorrect, the fault probably lies in the a.m. detector and muting stages of the I.F. Amplifier board or in the pre-amplifier and noise limiter stages of the F.M./C.W. Detector board.

25. If the audio stages are functioning correctly, select the FM mode and, using a suitably modulated signal, measure the audio and video outputs. Repeat the measurement for each i.f. bandwidth in turn.

26. Select the PULSE and CW modes in turn and make appropriate measurements as for para. 25.

27. If operation is unsatisfactory in either the CW, FM or PULSE modes, measure the control potentials, as given in Table 5 of Chap. 2, and the b.f.o. signal levels (Table 7 of Chap. 2). If the control levels of Table 7 (Chap. 2) are correct, the fault probably lies in the relevant section of the F.M./C.W. Detector board; alternatively the B.F.O. board is faulty. A malfunction of the Detector BFO TUNE control will be self-evident.

28. To check the 'tuning' meter facility, select the FM mode. Vary the frequency of the test signal and observe that the meter readings 'follow' correctly. If operation is unsatisfactory but the tests carried out in para. 25 were satisfactory, the fault lies in the meter-selection circuits of the F.M./C.W. Detector board.

29. Select the AM mode and note the presence of audio output (test signal suitably modulated). Measure the audio output from the I.F. Amplifier board and check that this output is zero (muted) in all modes except AM.

30. A malfunction of the AGC or manual IF GAIN controls implies a fault in the I.F. Amplifier board; this fault will also affect the 'S' meter readings (Chap. 2, para. 11).

AUXILIARY OUTPUTS

31. If the video output level is correct but neither of the audio outputs is obtained, the fault is in the F.M./C.W. Detector board (pre-amplifier, para. 17 of Chap. 2). If one of the audio output levels or the video output level is incorrect, the fault is in the Audio and Video Amplifier board; measure the signal levels as given in Table 9 of Chap. 2. A malfunction of the PHONES GAIN control will be self-evident.

32. Incorrect operation of the audio noise limiter implies a fault in the F.M./C.W. Detector board; check for a +12V control level at pin 4 of this board.

CHAPTER 6

DISMANTLING AND REASSEMBLY

WARNING

LETHAL VOLTAGES ARE GENERATED IN THIS EQUIPMENT, HENCE SWITCH OFF BEFORE DISMANTLING.

INTRODUCTION

1. The following instructions are sufficient to enable a faulty printed-wiring board or sub-assembly to be removed and replaced.

REMOVAL OF R.F. TUNER HEAD

2. (1) Twist the two winged Dzus fasteners in a counter-clockwise direction.

(2) Grip by the handle and withdraw.

DISMANTLING THE RECEIVER

Front Panel

3. (1) Remove the R.F. Tuner Head (para. 2).

(2) Loosen the two screws in the extension shaft of the tuning encoder knob; withdraw the knob-assembly.

(3) Remove the four screws holding the front-panel handles.

(4) Remove the six small screws securing the display bezel to the front panel.

(5) Remove the two screws at the top centre of the front panel.

(6) Invert the chassis and remove the row of screws (nearest front panel) which secure the narrow cover.

(7) Allow the front cover to drop down.

Removal of Sub-Assemblies - Underside (fig. 36)

4. All printed-wiring boards are secured by hexagonal nuts to pillars fixed to the chassis. With the exception of the Divider board, the Second Local Oscillator

board and the B.F.O. board, the connectors on all other boards are held in position by two slotted screws through one edge of the board.

(1) Remove all screws (20 plus 21) securing the two large covers.

(2) Unsolder any connecting leads to the board.

(3) If relevant, remove the two slotted screws (near one edge of board) holding the connector.

(4) Remove the hexagonal nuts securing the board to the chassis.

(5) Lift the board off the supporting pillars.

Removal of Sub-Assemblies - Top (fig. 35)

5. Printed-Wiring Boards. There are three plug-in boards viz the C.O.R./Serialiser/ Squelch board, the Battery Standby board and the A.F. and Video board.

6. Power Supply Assembly.

(1) Remove the Tuner Head (para. 2).

(2) Remove the two connectors.

(3) Remove the three screws securing the angle bracket to the chassis.

(4) Remove the three screws securing the assembly to the rear panel.

(5) Withdraw the assembly.

7. Dismantling the Power Supply Assembly is self-evident; access to most components is achieved by removing the top board (four screws) and the side component plate (four screws).

8. Display Assembly.

(1) Loosen the two screws in the extension shaft of the Tuning Encoder knob; withdraw the knob.

(2) Remove the two screws securing the top of the Display board.

(3) Unplug the board.

9. Frequency Standard Unit

(1) Remove the Tuner Head (para. 2).

(2) Unplug the unit.

10. Tuning Encoder Assembly

(1) Remove the Tuner Head (para. 2).

(2) Drop the front panel (para. 3).

(3) Unsolder all leads to the rear.

(4) Remove four screws through the rear support plate into the casting.

(5) Remove the three screws securing the support plate.

(6) Withdraw the assembly.

11. Logic Board

(1) Remove the Tuner Head (para. 2).

(2) Remove the six screws securing the cover.

(3) Remove the two screws holding the connector at the front edge of the board.

(4) Remove the four screws holding the two connectors along the left-hand edge of the board.

(5) Remove the three remaining screws securing the board to the casting.

(6) Unplug the board by lifting (slightly) the front edge and pulling towards the front panel.

REASSEMBLING THE RECEIVER

12. The instructions for reassembling the Receiver are the reverse to those given in para. 2 to 11.

CHAPTER 7

PERFORMANCE CHECKS

INTRODUCTION

1. This chapter provides a list of test equipment followed by those overall performance checks required to be carried out on a routine basis or following repair; also included are performance checks on the MA.2092C Signal Display Unit when used in conjunction with the Receiver.

TEST EQUIPMENT

2. Table 1 is a list of test equipment required for the checks in this chapter and for the fault-finding procedures in Chapter 5.

TABLE 1

Test Equipment

Item	Description
1	20-1000 MHz a.m./f.m. signal generator e.g. Marconi TF2006 fully equiped with plug-in modules.
2	20-1000 MHz a.m./pulse signal generator e.g. Marconi TF801D
3	Synthesised signal generator e.g. Racal 9061/62
4	Frequency counter, up to 5 MHz with 1 part in 10^9 stability e.g. Racal 9025
5	A.F. wattmeter e.g. Marconi TF2500
6	R.F. Voltmeter e.g. Racal 301A
7	100 Hz-8000 Hz distortion factor meter e.g. Marconi TF142F
8	Pulse generator to modulate item 2 e.g. Advance P655.
9	Spectrum analyser e.g. Hewlett Packard 141T Display with 8554B R.F. Section and 8552A or B I.F. Section.
10	Test Lead Racal ATG 5001
11	Oscilloscope with 30 MHz bandwidth and 10 mV/cm sensitivity e.g. Hewlett Packard 1701A

TABLE 1 (Cont'd)

Item	Description
12	100 Hz to 300 kHz signal generator e.g. Racal-Airmec 252.
13	Noise diode e.g. Magnetic AB Type 125A
14	Three-port combiner unit with 6 dB insertion loss e.g. Microlab Type FXR-DA3FB
15	FRO Test Unit Racal ATG5003
16	Multimeter e.g. AVO 9SX

PERFORMANCE CHECKS

3. The following performance checks apply to all frequency bands and assume that an R.F. Tuner Head is plugged into position.

Functional Checks

4. It is assumed that a 90 to 400 MHz R.F. Tuner Head is in use.

(1) Set the RANGE switch to 90-195 MHz.

(2) Before switching on, set the Receiver front-panel controls as follows:

(a) AGC switch to ON.

(b) MODE switch to AM.

(c) IF BANDWIDTH switch to 20 kHz.

(d) IF GAIN control to mid-position.

(e) NL switch to OFF.

(f) Meter switch to TUNE.

(g) FAST pushbutton depressed.

(h) COR switch to OFF.

(j) GAIN (a.f.) control to mid-position.

(k) BFO TUNE control to mid-position.

(3) Set the POWER switch to ON.

(4) Check that the SYN LOCK lamp glows.

(5) Check that the frequency displayed is 195.499 MHz.

(6) Spin the Tuning control in a counter clockwise direction until the changing frequency display stops; the frequency displayed must not be below 089.499.

(7) Set the RANGE switch to 195-400 MHz.

(8) Check that the SYN LOCK Lamp is still glowing.

(9) Check that the frequency displayed is 194.499 MHz.

(10) Spin the Tuning control in a clockwise direction until the changing-frequency display stops; the frequency displayed must not be above 400.499.

(11) Spin the Tuning control (counter-clockwise) to an arbitrary midband frequency; note the frequency display.

(12) Connect the Test Panel (item 15, Table 1) to the BCD OUTPUT socket on the rear (SKT1).

(13) Set the receiver RANGE switch to 195-400 MHz.

(14) Tune the receiver to 399.499 MHz, and check that the display on the Test Panel also shows 399.499.

(15) Set the POWER switch to STBY and then return it to ON; note that the frequency reading displayed has not changed.

5. The following checks cover the Signal Display Unit (S.D.U.) when used in conjunction with the receiver.

(1) Before switching on, set the S.D.U. front-panel controls as follows:-

(a) WIDTH switch to 3 MHz.

(b) DISPLAY switch as appropriate.

(c) FOCUS control to mid-position.

(d) BRILLIANCE control to mid-position.

(e) CENTERING control to mid-position.

(f) CENTRE MARKER switch to ON.

(g) CENTRE MARKER AMPLITUDE control to mid-position.

(h) AMPLITUDE control fully clockwise.

(2) Set the POWER switch on the SDU to ON.

(3) Adjust the FOCUS and BRILLIANCE controls to provide a clear trace.

(4) Connect a signal generator (item 1, Table 1) to the RF INPUT socket of the receiver.

(5) Set the signal generator to 150 MHz and 44 μV output.

(6) Tune the receiver to 150 MHz.

(7) Observe the signal on the SDU trace, and adjust the S.D.U. AMPLITUDE control as necessary.

(8) Move the receiver Tuning control in a clockwise direction and observe that the displayed signal moves to the left.

(9) Using the Tuning control and observing the frequency displayed, check that the width of the trace is approximately 3 MHz.

(10) Repeat operation (9) for the 1, 0.3 and 0.1 positions of the WIDTH switch.

(11) Reset the WIDTH switch to 3 MHz.

(12) Set the AMPLITUDE control to the maximum clockwise position.

(13) Set the signal generator output level to 1 μV.

(14) Observe that the signal amplitude on the trace is at least one quarter f.s.d.

(15) Increase the signal generator output level to 10 μV.

(16) Set the AMPLITUDE control to provide a signal amplitude of one quarter f.s.d.

(17) Increase the signal generator output level by 50 dB.

(18) Tune the receiver across the band, and check that the amplitude of any spurious signals appearing is not greater than one quarter f.s.d.

(19) Amplitude - modulate the signal generator with a 1 kHz tone.

(20) Check for a 1 kHz tone from the loudspeaker, and check the operation of the GAIN control on the SDU.

(21) Disconnect the signal generator.

(22) Set the CENTRE MARKER switch to ON.

(23) Observe the presence of a marker signal on the trace, and check the operation of the CENTRE MARKER AMPLITUDE control.

6. If the above tests are to be carried out using a 20-90 MHz or 400-1000 MHz Tuner Head, Table 2 gives the relevant tuning and range data for carrying out the instructions in para. 4 and 5.

TABLE 2

Signal Frequency Settings

Range	20-40 MHz	40-90 MHz	400-650 MHz	650-1000 MHz
Para.				
4(5)	40.499	-	650.499	-
4(6)	19.499	-	399.499	-
4(9)	-	39.499	-	649.499
4(10)	-	90.499	-	999.999
5(5)	30	50	500	800
5(6)	30	50	500	800
5(26)	40.499	90.499	650.499	999.999

Oscillator Stability

7. The equipment must have been in the 'off' condition for at least one hour before carrying out the following test.

(1) Withdraw the receiver on its runners.

(2) Remove the large bottom plate.

(3) Identify the divider board.

(4) Connect a frequency counter (item 4, Table 1) to the 5 MHz output terminal on the divider board.

(5) Set the POWER switch on the Receiver to ON, and note the time of day.

(6) After 45 minutes, note the frequency indicated by the counter, and check that it is within the limits of 4,999,998 MHz and 5,000,002 MHz.

(7) Remove the counter, refit the bottom plate and push the receiver back into the cabinet. Secure the Dzus fasteners.

Video Response

8. (1) Set the POWER switch to ON.

(2) Set the controls as follows:

(a) IF GAIN to mid-position.

(b) IF BANDWIDTH to 300 kHz.

(c) MODE to AM.

(d) SLOW pushbutton depressed.

(e) NL switch to OFF.

(f) AGC switch to ON.

(g) COR switch to OFF.

(h) Meter switch to TUNE.

(3) Connect the r.f. signal generator (item 3, Table 1) to the RF INPUT socket on the Receiver.

(4) Set the MODULATION FREQUENCY switch on the signal generator to EXT.

(5) Connect the a.f. signal generator (item 12, Table 1) to the EXT.MOD INPUT socket on the front panel of the r.f. signal generator.

(6) Set the RANGE switch to the required position.

(7) Tune the r.f. signal generator to the frequency shown in Table 3 and for an output level of 44 μV.

(8) Adjust the a.f. signal generator for a modulating frequency of 1 kHz and an output level of 500 mV.

(9) Adjust the modulation level control on the r.f. signal generator for a meter deflection of 70%.

(10) Connect the r.f. voltmeter (item 6, Table 1) to the VIDEO OUTPUT socket; set for a 75 ohm input.

TABLE 3

R.F. Signal Generator Frequency Setting

Range MHz	Frequency Setting MHz
20-40	30
40-90	50
90-195	145
195-400	300
400-650	500
650-1000	800

(11) If necessary, retune the receiver and check that the voltmeter reading is not less than 1 volt r.m.s.

(12) Check that the tuning meter is functioning correctly.

(13) Vary the modulating frequency from 100 Hz to 150 kHz, and check that the voltmeter reading does not vary by more than 6 dB; ensure that the modulation depth and signal generator output level are maintained throughout the measurements.

(14) Using an oscilloscope (item 11, Table 1), check the modulation depth at the IF OUTPUT socket.

A.M. Sensitivity

9. The following measurement is made with the condition as set up in para. 8.

(1) Set the modulation depth and frequency to 50% and 1 kHz respectively.

(2) Connect the Test Lead (item 10, Table 1) to SKT3 on the rear of the receiver.

(3) Connect the a.f. Wattmeter (item 5, Table 1) to terminals 1 and 2 on the Test Lead.

(4) If necessary, retune the receiver.

(5) Reduce the signal generator output level to 7 μV, and note the voltmeter reading (S + N).

(6) Switch off the 1 kHz modulating signal, and again note the voltmeter reading (N).

(7) Record (S + N)/N which should be greater than 10 dB.

(8) Repeat operations (5) to (7) for the remaining three bandwidths adjusting the r.f. generator output level in each case to that shown in Table 4.

TABLE 4

R.F. Signal Generator Level Settings

Bandwidth	Output Level
50 kHz	4.6 μV
20 kHz	2.9 μV
6 kHz	1.6 μV

(9) Increase the r.f. generator output level to 1 mV and the modulation depth to 80%.

(10) Set the IF BANDWIDTH switch to 50 kHz.

(11) Note the voltmeter reading (S + N).

(12) Switch off the modulation and again note the voltmeter reading (N).

(13) Record (S + N)/N which should be greater than 40 dB.

Audio Response

10. The following measurement is made with the conditions set up in para. 9.

(1) Set the IF BANDWIDTH switch to 300 kHz.

(2) If necessary, retune the receiver.

(3) Set the r.f. signal generator for an output level of 44 μV and 50% modulation at 1000 Hz.

(4) Note the a.f. wattmeter readings whilst increasing the modulation frequency to 20 kHz; ensure that generator output level and modulation depth are maintained constant. The audio output level should not vary by more than 3 dB and should never be less than 15 mW (into 200Ω).

(5) Connect the a.f. wattmeter to terminals 3 and 4 on the Test Lead, and repeat operation (4). The output level should never be less than 1 mW (into 600Ω).

(6) Connect the a.f. wattmeter to terminals 5 and 6 on the Test Lead, and repeat operation (4). The output level should never be less than 1 mW (into 600Ω).

C.O.R. Sensitivity

11. The following measurement is made with the conditions set up in paragraph 10.

(1) Transfer the Test Lead from SKT3 to SKT2 (COR) on the rear.

(2) Reconnect the Audio lead to SKT3.

(3) Connect a multimeter (item 16, Table 1) to terminals 1 and 2 of the Test Lead.

(4) Set the multimeter to an ohms range.

(5) Set the COR switch to SET LEVEL.

(6) Set the COR LEVEL control to the maximum clockwise position.

(7) Reduce the r.f. generator output level to 1 mV and check the receiver tuning.

(8) Check that the COR Lamp is glowing, that the Multimeter indicates a short-circuit, and that audio output is present.

(9) Set the r.f. generator MODE switch to OFF.

(10) Check that the COR Lamp is extinguished, that the Multimeter indicates an open-circuit, and that audio output is muted.

(11) Set the COR switch to DELAY.

(12) Reset the r.f. generator MODE switch to AM 0-100%, checking on the multimeter for a short-circuit.

(13) Again, set the r.f. generator MODE switch to OFF and check that the open-circuit indication on the Multimeter occurs between 5 and 10 seconds later, but that no delay occurs for audio muting.

I.F. Output

12. (1) Remove the r.f. signal generator (item 3, Table 1) and connect in its place the a.m./f.m. signal generator (item 1, Table 1).

(2) Set the a.m./f.m. generator for 44 μV, c.w. output.

(3) Connect the r.f. voltmeter (item 6) to the IF OUTPUT socket on the rear (SKT4).

(4) Set the MODE switch to CW.

(5) If necessary, retune the receiver.

(6) Check that the r.f. voltmeter reading is 20 mV minimum (into 75Ω).

Manual I.F. Gain Control and 'S' Meter

13. The following measurement is made with the conditions set up in paragraph 12.

(1) Set the AGC switch to ON.

(2) Set the IF BANDWIDTH switch to 20 kHz.

(3) Set the receiver Meter switch to 'S'.

(4) Reduce the generator output level to 1 μV.

(5) Set the IF GAIN control until the r.f. voltmeter reads 20 mV.

(6) Increase the generator output level to 10 mV.

(7) Adjust the IF GAIN control for a reading of 20 mV on the r.f. voltmeter.

(8) Check the 'S' meter reading is 10 mV ± 10 dB.

F.M. Sensitivity

14. The following measurement is made with the conditions set up in paragraph 13.

(1) Transfer the Test Lead from SKT2 to SKT3 on the rear.

(2) Reconnect the COR Lead to SKT2.

(3) Connect the r.f. voltmeter to terminals 1 and 2 of the Test Lead.

(4) Set the MODE switch to FM and AGC switch to ON.

(5) Set the IF BANDWIDTH switch to 6 kHz.

(6) Set the a.m./f.m. generator output level to 1.4 μV with 2 kHz deviation and modulated at 1 kHz.

(7) Tune the receiver and note the r.f. voltmeter reading (S + N).

(8) Switch off the modulation and again note the r.f. voltmeter reading (N).

(9) Record (S + N)/N which should not exceed 20 dB.

(10) Repeat operation (5) to (9) with the bandwidth, deviations and levels given in Table 5.

TABLE 5

Test Equipment Settings: F.M. Sensitivity

Receiver IF BANDWIDTH kHz	Deviation kHz	Generator Output Level μV
20	7	2.6
50	17	4.1
300	100	10.0

(11) Reset the IF BANDWIDTH switch to 50 kHz.

(12) Increase the generator output level to 1 mV and switch on the modulation.

(13) Set the deviation to 25 kHz.

(14) Note the r.f. voltmeter reading (S + N).

(15) Switch off the modulation and again note the r.f. voltmeter reading (N).

(16) Record (S + N)/N which should be greater than 40 dB.

Noise Factor

15. The following measurement is made under the conditions set up in paragraph 14.

(1) Connect the a.f. wattmeter to terminals 1 and 2 of the Test Lead.

(2) Set the controls as follows:

(a) MODE switch to CW.

(b) IF BANDWIDTH switch to 50 kHz.

(c) AGC switch to OFF.

(d) NL switch to OFF.

(3) Connect the noise source (item 13, Table 1) to the RF INPUT socket.

(4) Tune the receiver to the frequency shown in Table 6 for the appropriate range. Note the change in audio output level with the diode source switch on and off. Refer to diagram below in order to obtain the noise factor.

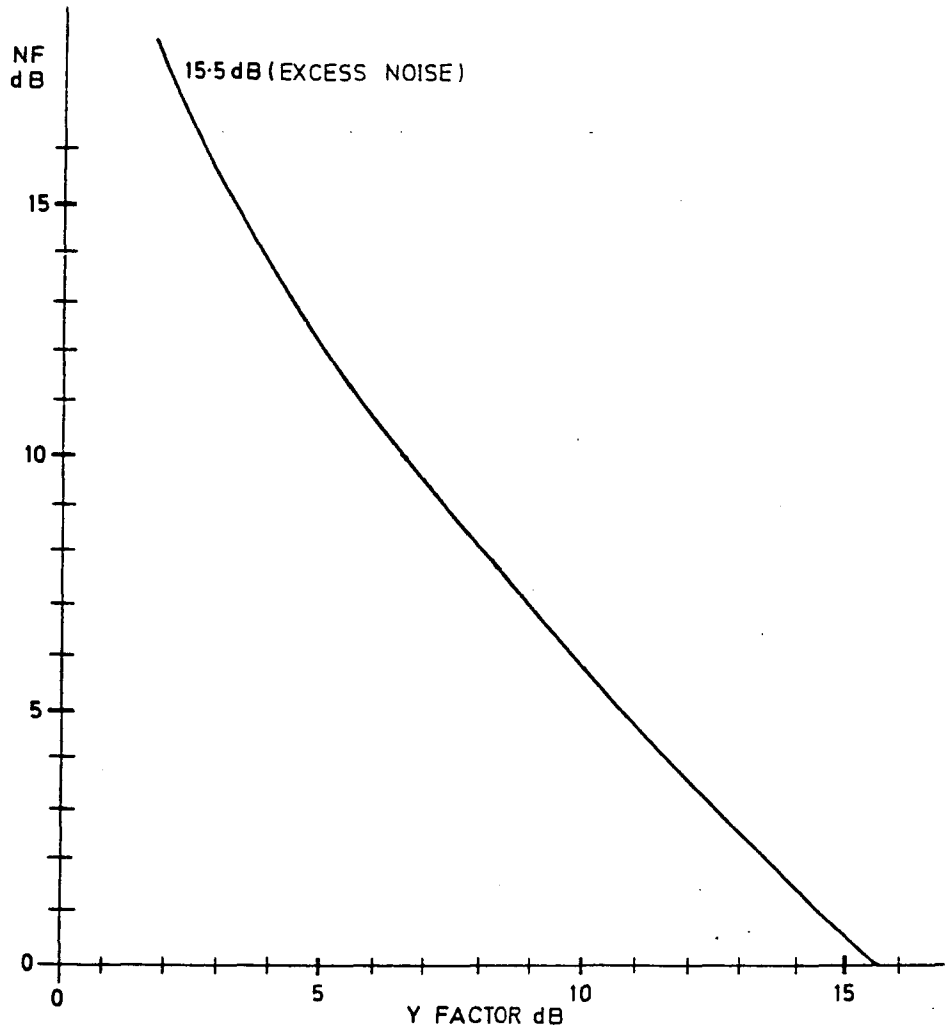


TABLE 6

Test Frequencies: Noise Factor

Range	Receiver Tuned Frequencies MHz
20–40	30
40–90	60
90–195	150
195–400	300
400–650	500
650–1000	800

B.F.O.

16. The following measurement is carried out under the conditions of paragraph 15.

(1) Disconnect the a.f. wattmeter and connect a frequency counter (item 4, Table 1) to terminals 1 and 2 of the Test Lead.

(2) Set the controls as follows:

(a) MODE switch to CW.

(b) IF BANDWIDTH switch to 20 kHz.

(c) BFO TUNE control to the centre position.

(d) Meter switch to 'S'.

(3) Set the a.m./f.m. generator output level to 10 μV.

(4) Tune the receiver to the generator frequency and for a peak reading on the 'S' meter.

(5) Note the frequency counter display.

(6) Turn the BFO TUNE control, in turn, to its maximum clockwise and counter clockwise settings. Note that the frequency displayed rises by at least 10 kHz at each extreme setting.

Noise Limiter

17. The following measurement is carried out under the conditions of paragraph 16.

(1) Disconnect the frequency counter and connect an oscilloscope to terminals 1 and 2 of the Test Lead.

(2) Set the MODE switch to AM and the NL switch to OFF.

(3) Amplitude-modulate the signal generator with 1 kHz at 70%.

(4) Set the output level of the generator to 44 μV.

(5) Observe the audio waveform on the oscilloscope.

(6) Set the NL switch to ON, and observe that clipping of the displayed waveform is occurring.

I.F. Bandwidth

18. The following measurement is carried out under the conditions of paragraph 17.

(1) Disconnect the a.m./f.m. generator (item 1) and connect the a.m./pulse generator (item 2, Table 1) to the RF INPUT socket.

(2) Amplitude-modulate the generator at 1 kHz and a depth of 50%.

(3) Disconnect the oscilloscope and connect the r.f. voltmeter to terminals 1 and 2 of the Test Lead.

(4) Set the generator frequency to 30 MHz and output level to 100 μV.

(5) Set the receiver controls as follows:

(a) AGC switch to ON.

(b) IF BANDWIDTH switch to 6 kHz.

(6) Observe the r.f. voltmeter indication.

(7) Set the AGC switch to OFF.

(8) Adjust the IF GAIN control for a voltmeter indication as in (6) above.

(9) Tune the receiver across the passband, and note the frequencies at which the voltmeter indication drops by 3 dB.

(10) Repeat the above procedure for the 20 kHz, 50 kHz and 300 kHz bandwidths; check that, in each case, the bandwidth is within 20% of nominal.

Pulse Signals ('B' Test)

19. The following measurement is carried out under the conditions of paragraph 18.

(1) Set the receiver controls as follows:

(a) MODE switch to PULSE.

(b) AGC switch to ON.

(c) IF BANDWIDTH switch to 300 kHz.

(2) Pulse-modulate the generator at 1 kHz with a pulse width of 10 µs; use the pulse generator (item 8, Table 1).

(3) Connect the oscilloscope to the VIDEO OUTPUT socket (SKT6).

(4) Set the generator frequency as appropriate and the output level to 100 µV.

(5) Check that the displayed video signal has a rise-time (10%-90%) of not greater than 20 µs.

Local Oscillator Radiation

20. (1) Remove all previously connected test equipment.

(2) Set the Receiver controls as follows:

(a) IF GAIN control to its mid-position.

(b) IF BANDWIDTH switch to 300 kHz.

(c) MODE switch to CW.

(d) FAST pushbutton depressed.

(e) NL switch to OFF.

(f) AGC switch to ON.

(g) COR switch to OFF.

(h) Meter switch to TUNE.

(3) Connect the spectrum analyser (item 9, Table 1) to the RF INPUT socket.

(4) Set the controls on the spectrum analyser in accordance with the relevant manual.

(5) Tune the receiver to the frequencies given in Table 7, and check that for each range the radiation level does not exceed 10 μV e.m.f.

(6) Disconnect the test equipment.

TABLE 7

Receiver Settings: Oscillator Radiation

Range MHz	Receiver Tuned Frequencies MHz
20 - 40	20, 30 and 40
40 - 90	40, 60 and 90
90 - 195	90, 150 and 195
195 - 400	195, 300 and 400
400 - 650	400, 500 and 650
650 - 1000	650, 800 and 1000

CHAPTER 8

POST-REPAIR ADJUSTMENTS

INTRODUCTION

1. The adjustments given in this chapter are to be carried out, where relevant, following a repair to a sub-assembly within the receiver. Following the adjustments, the relevant performance checks given in Chap. 7 are to be carried out.

TEST EQUIPMENT

2. Refer to Table 1 for a list of test equipment required.

TABLE 1

Test Equipment

Item Ref. No.	Description
1	Oscilloscope, e.g. Hewlett Packard 1701A.
2	20-1000 MHz signal generator, e.g. Marconi TF2006, fully equiped with plug-in modules.
3	Amplitude modulator, Marconi TM 9897A.
4	Audio signal generator, e.g. Advance J3.
5	Frequency Counter, e.g. Racal 9025.
6	A.F. Wattmeter e.g. Marconi TF2500

ADJUSTMENTS

3. A serviceable Head-Tuner must be plugged into the main Receiver in order to carry out the following adjustments.

Tuning Encoder

4. (1) Connect an oscilloscope to pin 4 of the potentiometer board at the rear of the Tuning Encoder (fig. 16).

(2) Switch on the receiver.

(3) Spin the tuning control and adjust R2 on the board for a 6V p-p display.

(4) Connect the oscilloscope to pin 10 of the board and, with the tuning control spinning, adjust R1 for a 6V p-p display.

Audio Output Levels

5. (1) Ensure that the receiver is switched off.

(2) Connect the amplitude modulator and audio signal generator to the r.f. signal generator.

(3) Connect the output of the r.f. signal generator to the antenna input socket on the Head-Tuner.

(4) Set the r.f. generator output to 30.500 MHz and 5 µV e.m.f.

(5) Set the modulating frequency to 1 kHz for both a.m. and f.m.

NOTE: The amplitude modulator has an insertion loss of 20 dB.

(6) Switch on the receiver and check that the SYN LOCK lamp is glowing.

(7) Tune the receiver to 30.500 MHz.

(8) Connect the oscilloscope probe to the junction of R21, D5, D6 on the F.M./C.W. Detector board (fig. 8).

(9) Apply 50% a.m. to the r.f. input signal; set the Receiver MODE switch to AM and the BANDWIDTH switch to 20 kHz.

(10) Adjust R24 on the I.F. Amplifier board (fig. 6) to give 1V p-p oscilloscope display.

(11) Set the receiver MODE switch to FM.

(12) Apply frequency modulation to the r.f. input signal. The required deviation for a given receiver bandwidth setting is given in Table 2.

(13) Referring to Table 2, adjust the preset controls on the FM/CW Detector board for a 1V p-p displayed signal.

TABLE 2

Adjustments to F.M./C.W. Detector Board

Receiver Bandwidth	Deviation kHz	Adjust:-
6	2	R6
20	7	R29
300	100	R40

(14) Set the r.f. generator for c.w. operation.

(15) Set the receiver MODE switch to CW.

(16) Offset the BFO control until a signal of suitable amplitude is displayed.

(17) Adjust R44 on the F.M./C.W. Detector board for a 1V p-p displayed signal.

(18) Terminate, at the rear of the receiver, each of the audio outputs with the load resistor given in Table 3.

TABLE 3

Adjustments to Video and Audio Amplifier Board

Output Level (mW)	Tolerance (mW)	Load Resistor (ohms)	Adjust:
100 (pins 1 and 2)	± 5	35	R5
30 (pins 3 and 4)	± 2	200	R2
2 (pins 5 and 6)	± 0.1	600	R4
2 (pins 7 and 8)	± 0.1	600	R3

(19) Using the AF wattmeter, and referring to Table 3, adjust each preset control (Video and Audio Amplifier board - fig. 12) to obtain an output level reading within the stated tolerance.

(20) Connect the r.f. voltmeter to the video output at the rear of the receiver; terminate with 75 ohms.

(21) Adjust R1 (Video and Audio Amplifier board) for a reading of 1.4V ± 0.05V r.m.s.

Frequency Standard

6. (1) Disconnect the coaxial lead from the Frequency Standard assembly.

(2) Connect a frequency counter to the output of the Frequency Standard.

(3) Remove the rubber plug in the top of the Frequency Standard.

(4) Using a suitable trimming tool, adjust the preset control for a frequency display of 5,000,000 ± 2 Hz.

Tuning Meter

7. (1) Set the BANDWIDTH switch to 300 kHz, and the meter switch to TUNE.

(2) Adjust T4 (F.M./C.W. Detector board) so that the tuning meter deflection is centred.

(3) Set the BANDWIDTH switch to 50 kHz and adjust L9 so that the tuning meter deflection is centred.

(4) Set the BANDWIDTH switch to 6 kHz and adjust L7 so that the tuning meter deflection is centred.

(5) Set the meter switch to 'S'.

(6) Reduce the r.f. generator output to 2 μV e.m.f. Check that the meter deflection is just above the left-hand graduation .

(7) Increase the r.f. generator output and observe that the meter deflects to the right.

(8) Switch off the receiver.

(9) Disconnect all test equipment.

CHAPTER 9

COMPONENTS LIST

Cct. Ref.	Value	Description	Rat.	Tol %	Racal Part Number	Manufacturer
SUB-ASSEMBLIES						
		R.F. Tuner 20 - 90 MHz				Racal DA501714
		R.F. Tuner 90 - 400 MHz				Racal DA501715
		R.F. Tuner 400 - 1000 MHz				Racal DA501729
		Tuning Encoder				Racal CA44180
		Logic				Racal BA502070
		Intermediate Logic				Racal BA502068
		Frequency Display				Racal BA502069
		Master Oscillator				Racal 9400
		Divider				Racal BA502073
		L.F. Loop				Racal BA501697
		Transfer Loop				Racal BA501750
		H.F. Loop				Racal BA501752
		2nd L.O.				Racal BA502075
		2nd Mixer and I.F. Filter				Racal BA502074
		I.F. Amplifier				Racal BA502187
		F.M./C.W. Detector				Racal BA502186
		B.F.O.				Racal BA502071
		Video and Audio Amplifier				Racal BA502067
		C.O.R./SER. Control				Racal BA502108
		Main Power Supply				Racal BA502185
		Battery-Standby Supply				Racal BA502109
CHASSIS-MOUNTED COMPONENTS						
1LP1-2		FAST Lamp				HY82512W
1LP3-4		SLOW Lamp				HY82512W
1LP5-6		HOLD Lamp				HY82512W
1LP7		Power 'on' lamp				Guest Int. 525B
1LP8		SYN LOCK lamp				Guest Int. 525B
1LP9		COR Lamp				Guest Int. 525B
D1		Diode			32-1601	Texas 1N4002
D2		Diode			32-1601	Texas 1N4002
D3		Diode			32-1601	Texas 1N4002
D4		Diode			32-1601	Texas 1N4002
D5		Diode			32-1601	Texas 1N4002

Cct. Ref.	Value	Description	Rat.	Tol %	Racal Part Number	Manufacturer
D6		Diode			32-1601	Texas 1N4002
D7		Diode			32-1601	Texas 1N4002
D8		Diode			32-0010	Mullard 0A47
D9		Diode			32-1601	Texas 1N4002
R1	2.2 kΩ	Resistor			30-4226	Electrosil TR4
R2	10 kΩ	IF GAIN			30-6026	Plessey MH-1
R3	100 kΩ	BFO TUNE			30-6027	Plessey MH-1
R4	10 kΩ	PHONES GAIN			30-6026	Plessey MH-1
R5	10 kΩ	COR LEVEL			30-6029	Plessey MH-1
R6	270Ω	Resistor			30-4127	Electrosil TR4
R7	1.2 kΩ	Resistor			30-1526	Mullard CR16
R8	3.9 kΩ	Resistor			30-1532	Mullard CR16
C1	1 µF	Capacitor			31-1213	ITT TAA 1M35A
C2	2.2 µF	Capacitor			31-1212	ITT TAA 2.2M20A
C3	2.2 µF	Capacitor			31-1212	ITT TAA 2.2M20A
C4	1 µF	Capacitor			31-1213	ITT TAA 1M35A
C35-C36	1000pF	Capacitor			31-6509	Erie 361
C38-51	330pF	Capacitor			31-1526	Erie 831/N5600
C52-55	0.1 µF	Capacitor			31-1602	Erie 811/T18V
C58, 59	0.01 µF	Capacitor			31-1667	ITW CKO58X103K
C60		Capacitor			31-6510	Erie 1216-001
C61	39 pF	Capacitor	200V	10%	31-1818	Erie N750/YD
FS1		(FUSE, 1A (115V)				Bulgin F286
		(FUSE, 0.5A (230V)			33-0080	Bulgin F286
SA		FAST switch			33-4105	Burgess H592103
SB		SLOW switch			33-4105	Burgess H562103
SC		HOLD switch			33-4105	Burgess H562103
SD		Meter switch			33-4104	Render R53005
SE		AGC switch			33-4103	
SF		MODE switch				Racal AD502191/4
SG		NL switch			33-4103	
SH		POWER switch				Racal AD502191/3
SK		IF BANDWIDTH-kHz switch				Racal AD502191/4

Cct. Ref.	Value	Description	Rat.	Tol %	Racal Part Number	Manufacturer
SJ		COR switch				Racal AD502191/1
PL1		Mains input plug/filter			33-3359	
		Free socket for PL1			33-3351	
SKT1		Serial data output socket			33-3265	Belling Lee L653/ S/AU
SKT2		COR output socket			33-3268	Belling Lee L654/ S/AU
SKT3		Audio output socket			33-3268	Belling Lee L654/ S/AU
SKT4		IF2 output socket			33-3259	Suhner 24BNC 50-1-1C
SKT5		IF1 output socket			33-3259	Suhner 24BNC 50-1-1C
SKT6		Video output socket			33-3259	Suhner 24BNC 50-1-1C
SKT7		PHONES jack socket			33-3273	Rendar R3262
SKT8		Connector			33-3252	Cannon DCMF 25W3S
T1		Transformer				Gardners VM7464
T2		Transformer				Gardners VM7464
X1		Regulator			32-4436	Fairchild UGJ 7805KC
X2		Regulator			32-4436	Fairchild UGJ 7805KC
FX1-16		Ferrite Bead			33-7157	Mullard FX1242
ME1		Meter				Racal AD50198
RLA/4		Relay (COR)			33-7533	Magnetic Devices SM5MH97
LP1-6		Lamp			33-0064	HY82512W
LP7-9		Lamp	5V		33-0065	Guest Int. 525B
		Encoder			51-2108	

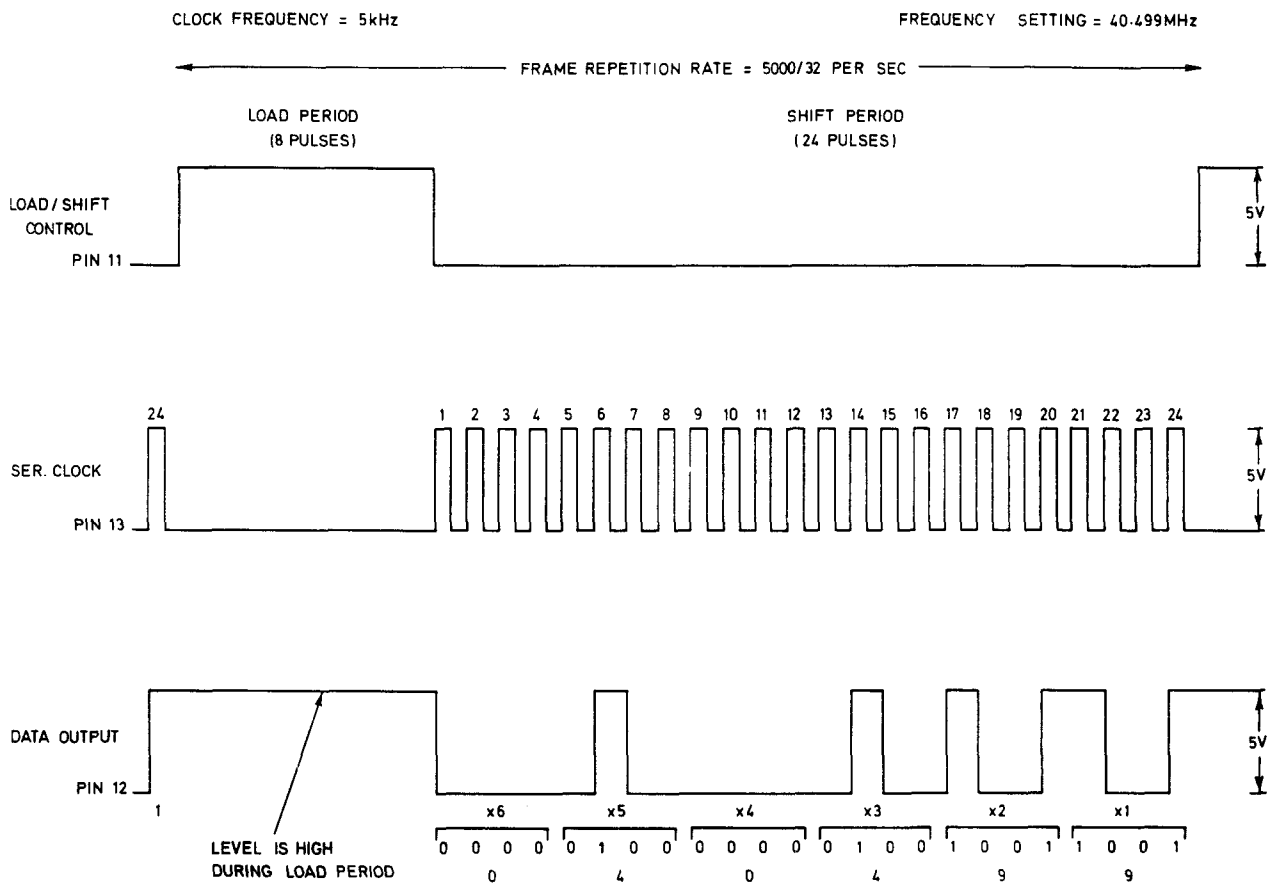
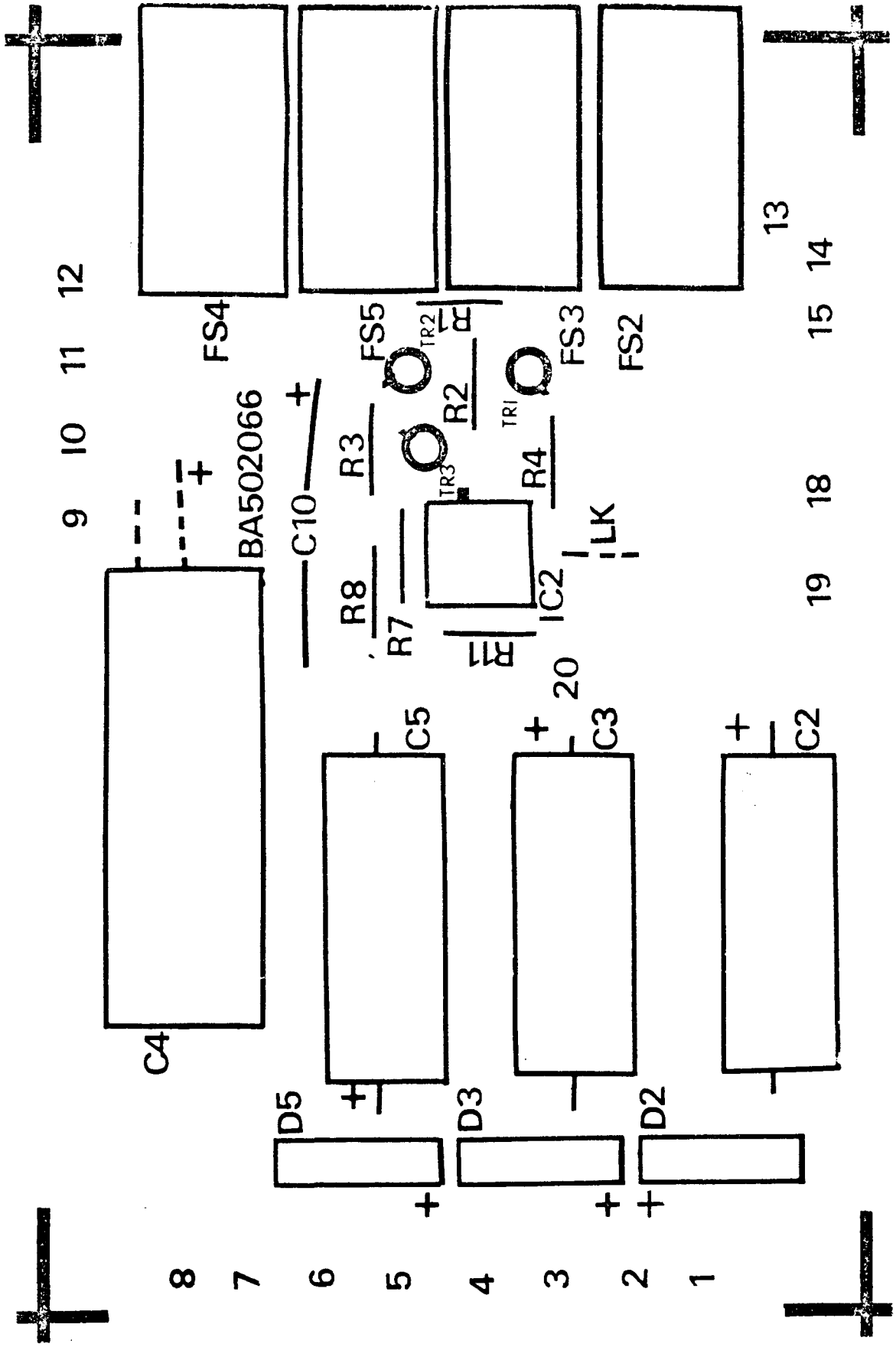
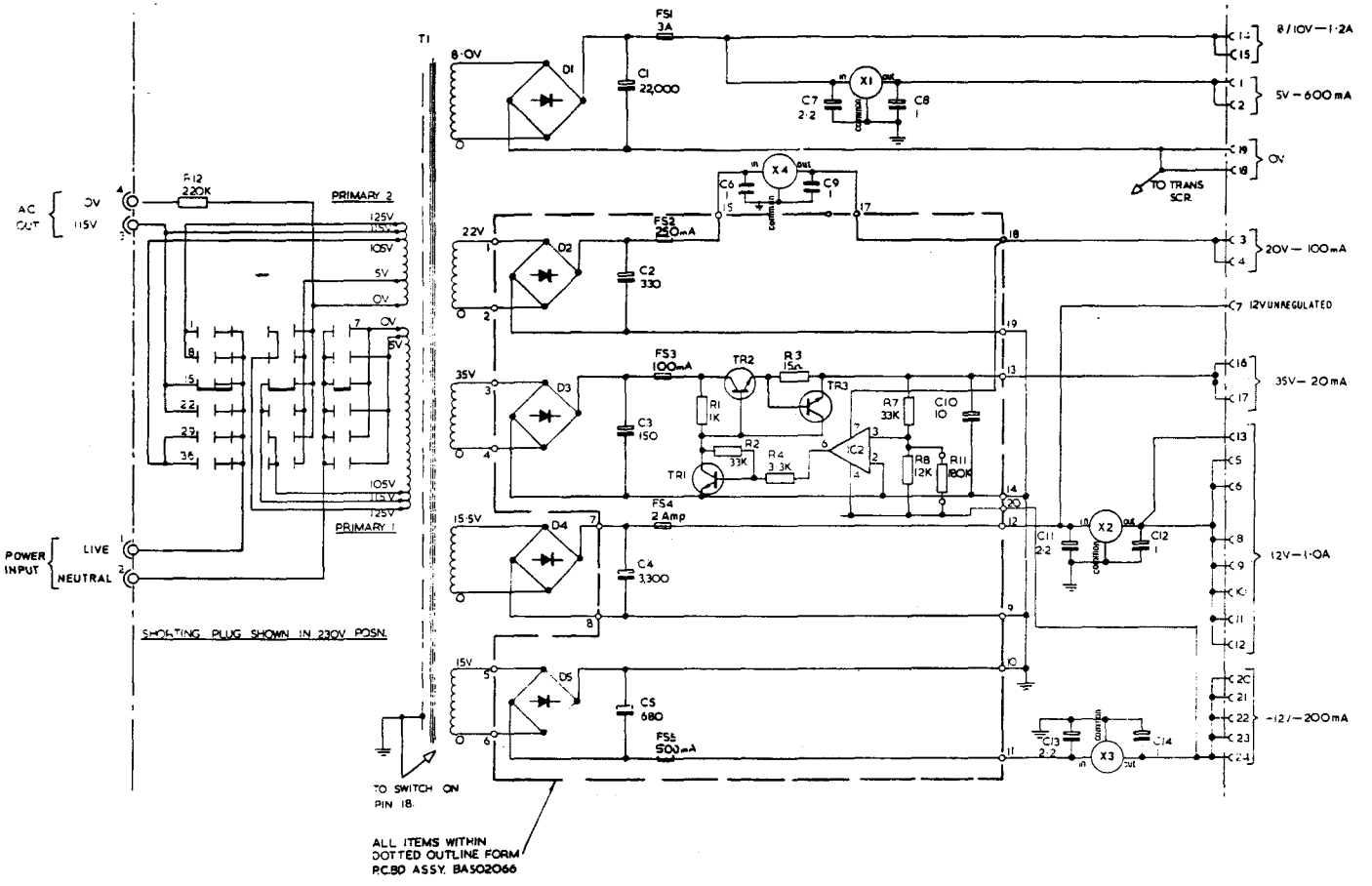


Fig.1 Serializer Timing Diagram



Component Layout: Receiver Power Supply Board

Fig. 2



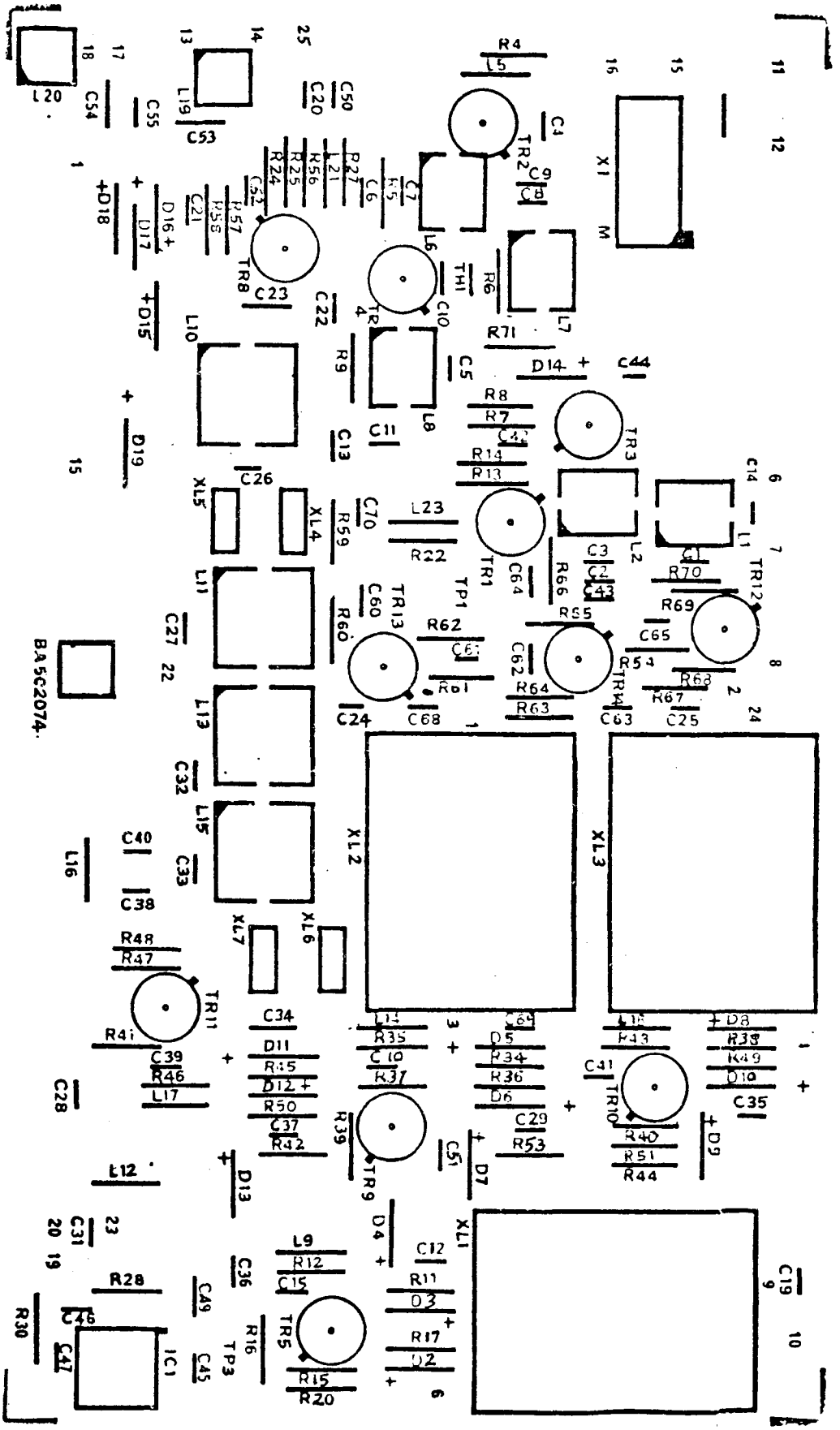
IC's
IC2 USB 7741393
DIODES
D2-D3,D5,BSBID1, SBO6 D4, SB
TRANSISTORS
TR1&3 BC107, TR2 40346.

VOLTAGE REGULATORS
X1 μA 7805 X2 uA7812
X3 LM 320K-12
X4 78M20UC

WOH 6245 CC 502185
7

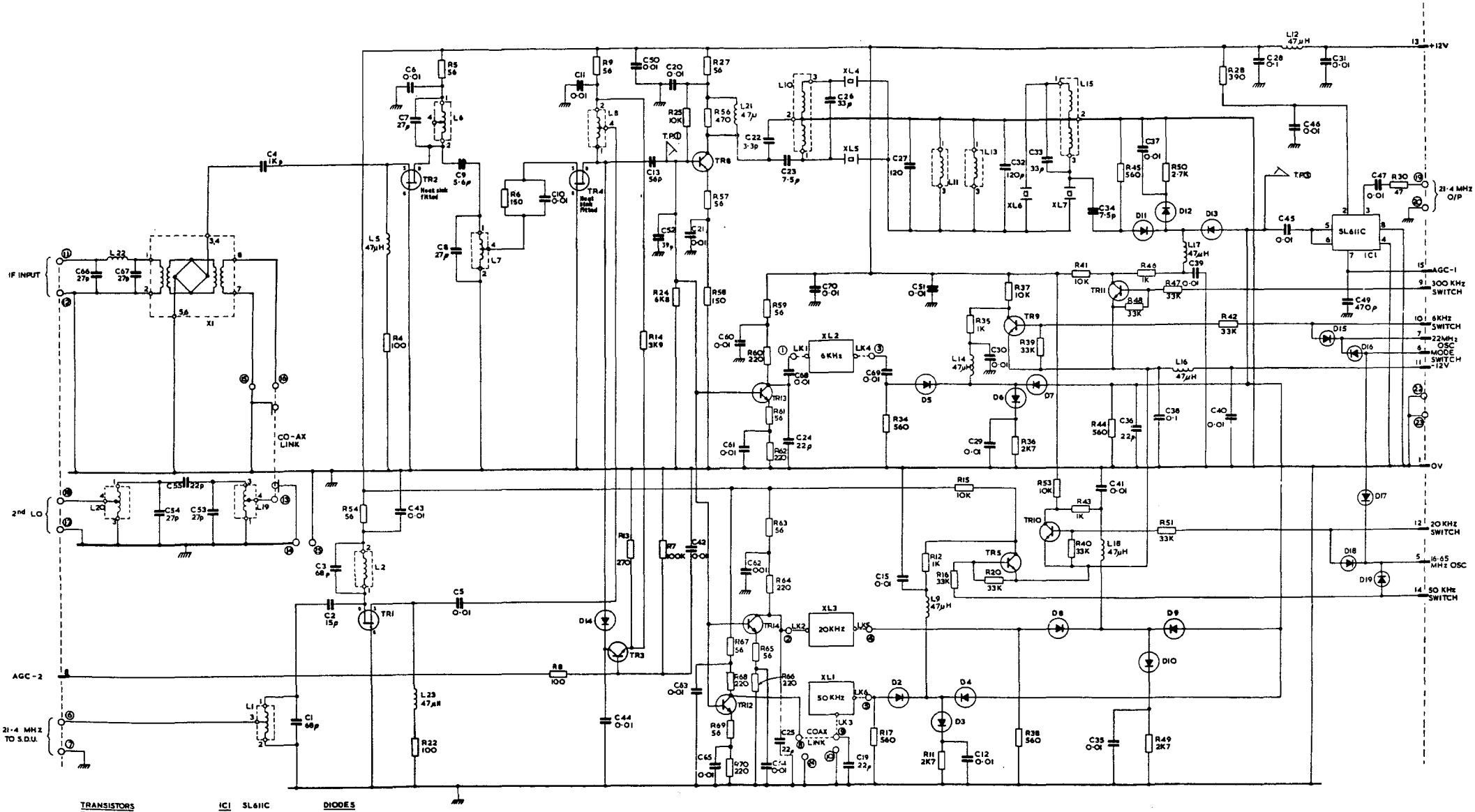
Circuit Diagram: Receiver Power Supply

Fig.3



Component Layout: 2nd Mixer and I.F. Filter Board

Fig. 4



TRANSISTORS
TR1 2 & 4 U310
TR3 BC 109
TR8, 12, 13, 14, 2N2369
TR5 9 10 & 11 BC 107

IC1 SL611C

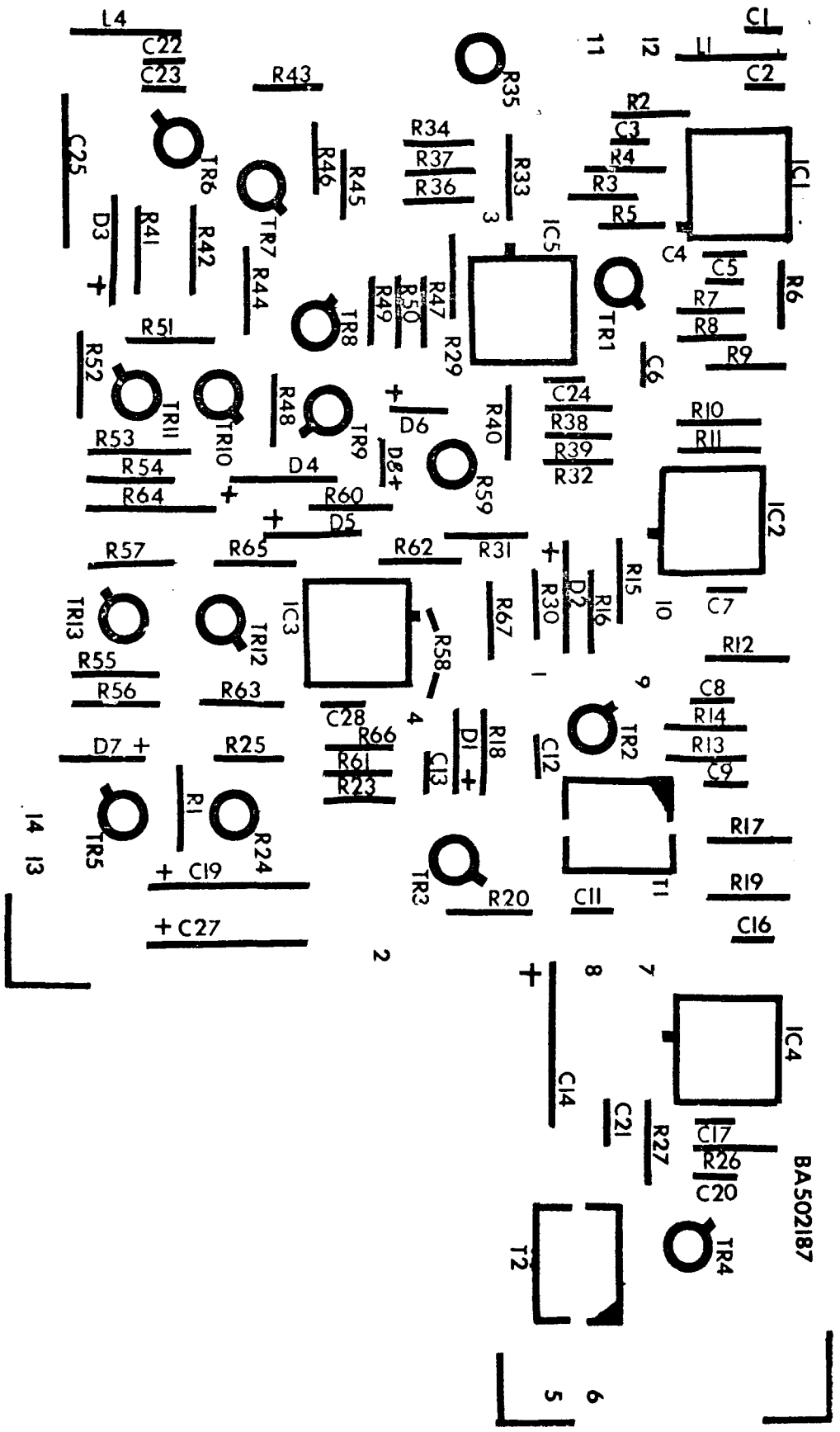
DIODES
D2-13, 15-19, ITT IN4149
D14 HEWLETT PACKARD 5082-3080

THERMISTER
TH1 MULLARD VA1109

WOH 6245 | DC 502074
19

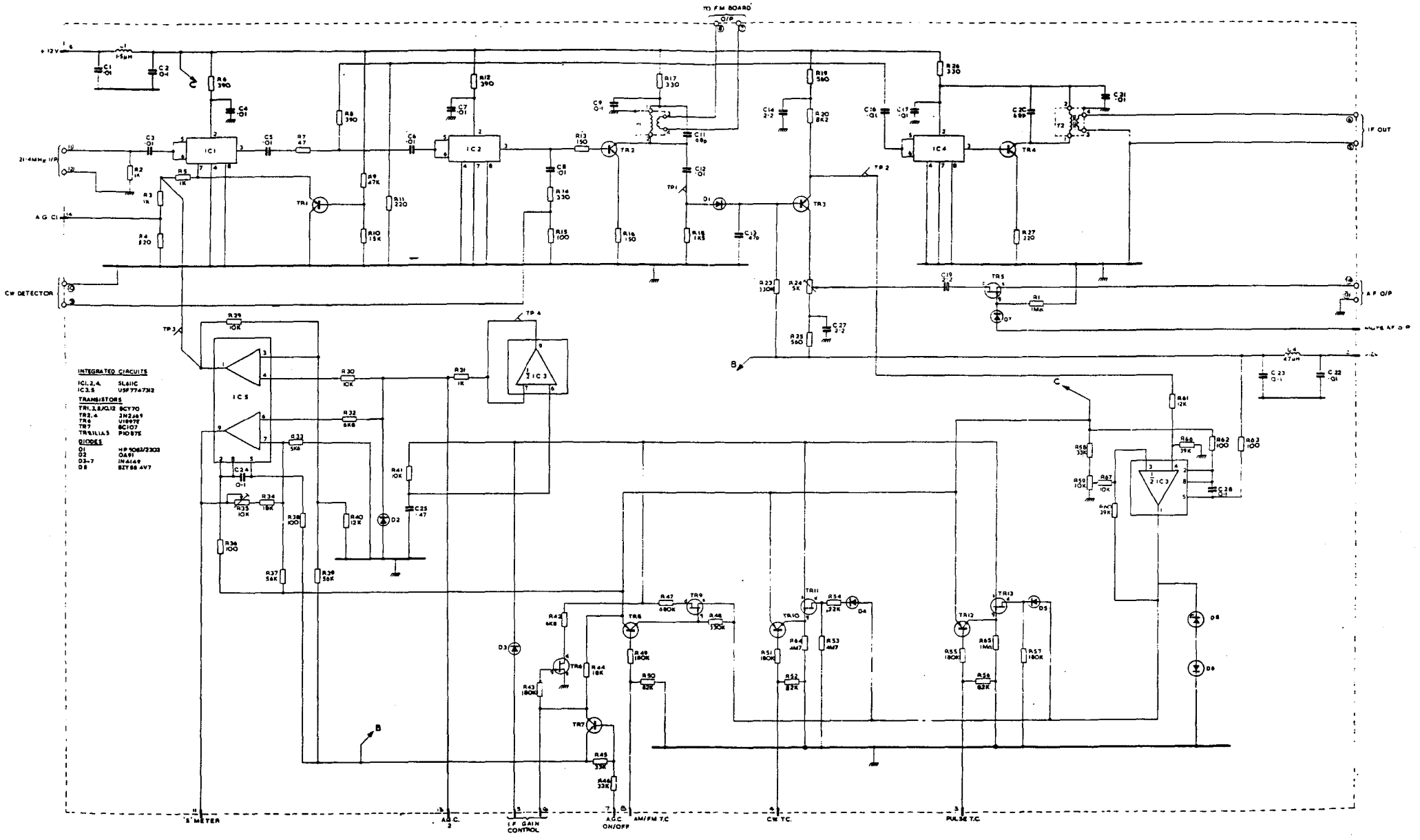
Circuit Diagram; 2nd Mixer and I.F. Filter Board

Fig. 5



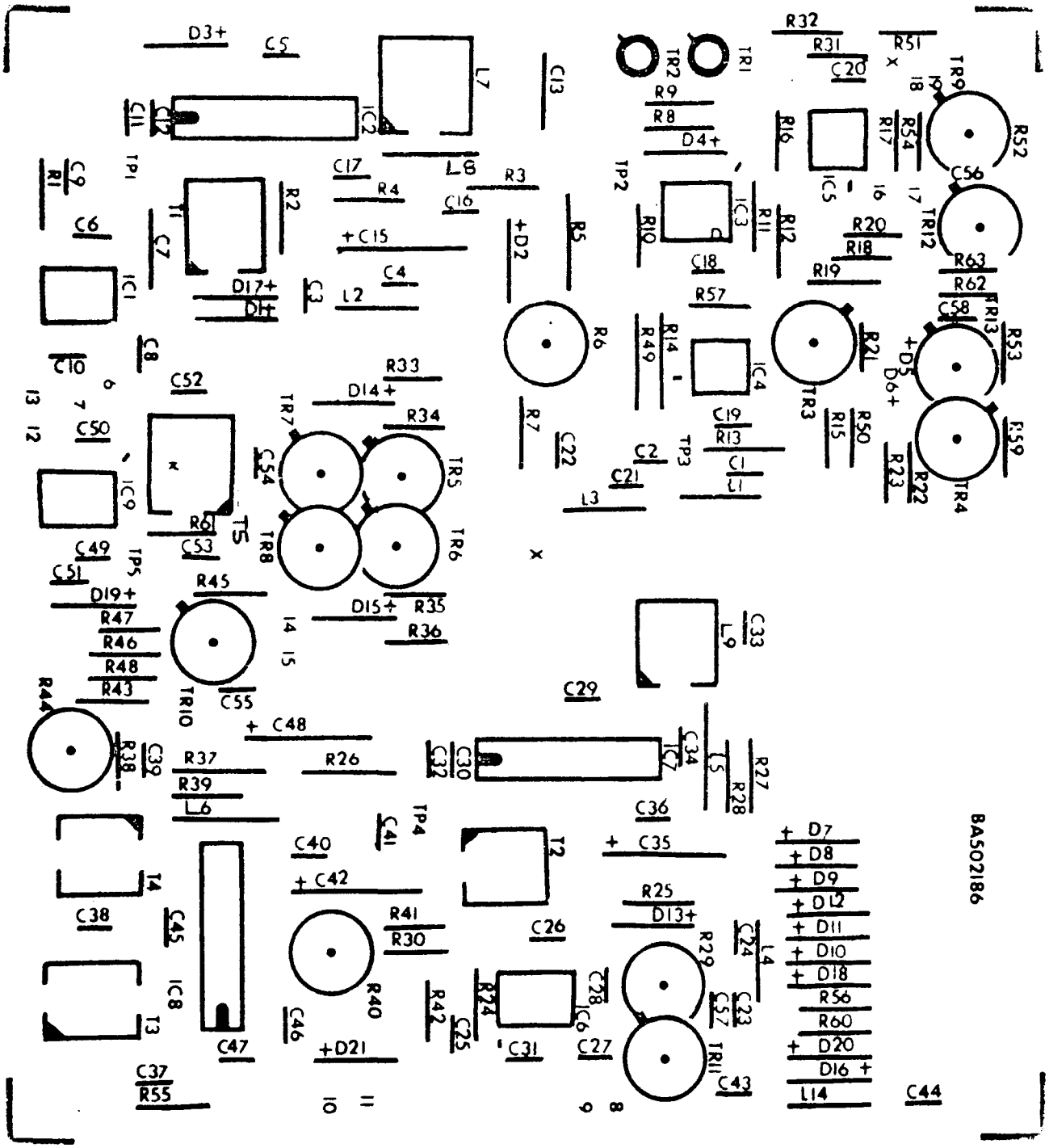
Component Layout: I.F. Amplifier and A.M./Pulse Detector Board

Fig. 6

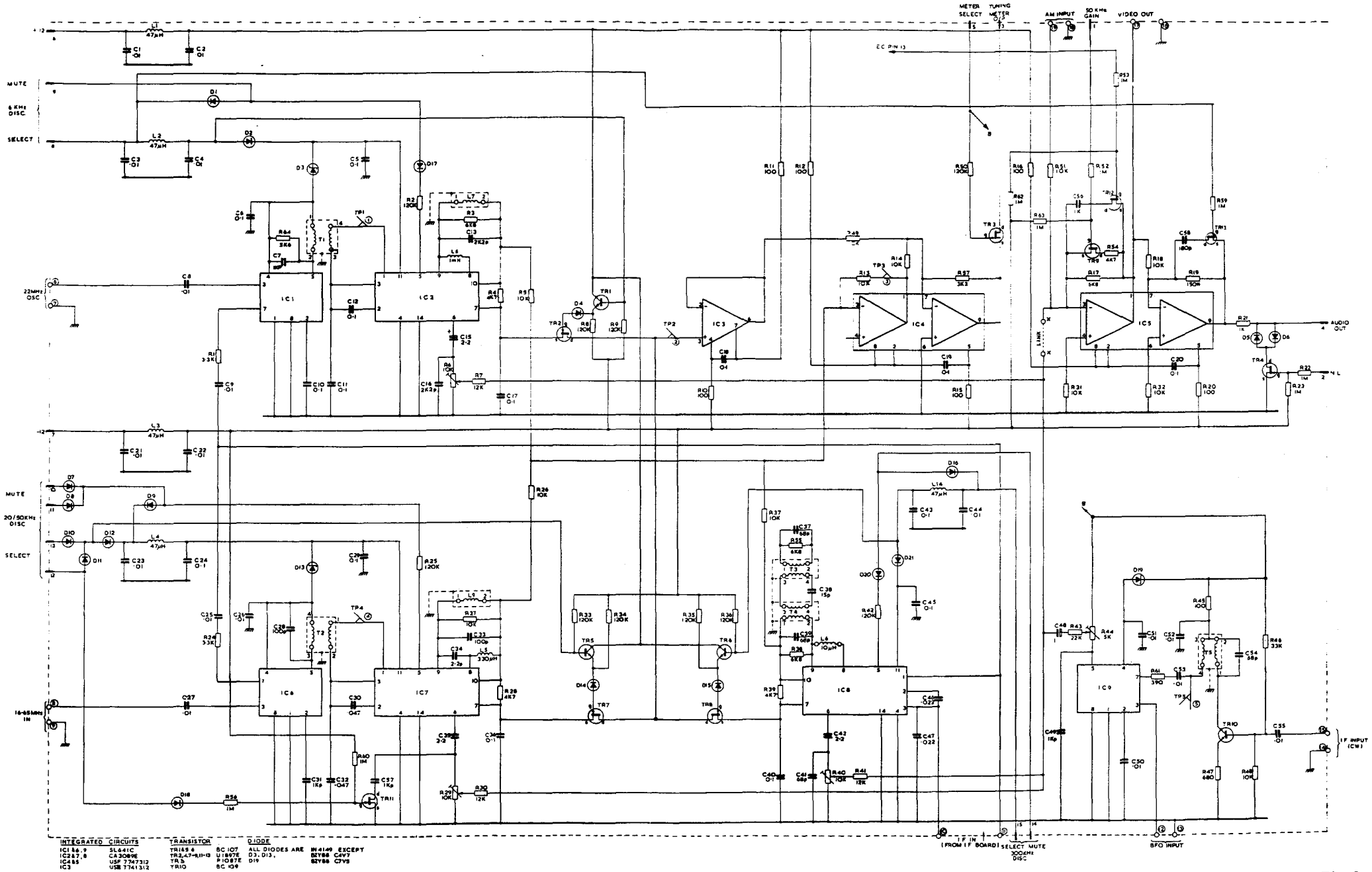


Circuit Diagram: I.F Amplifier and AM/Pulse Detector Board

Fig.7



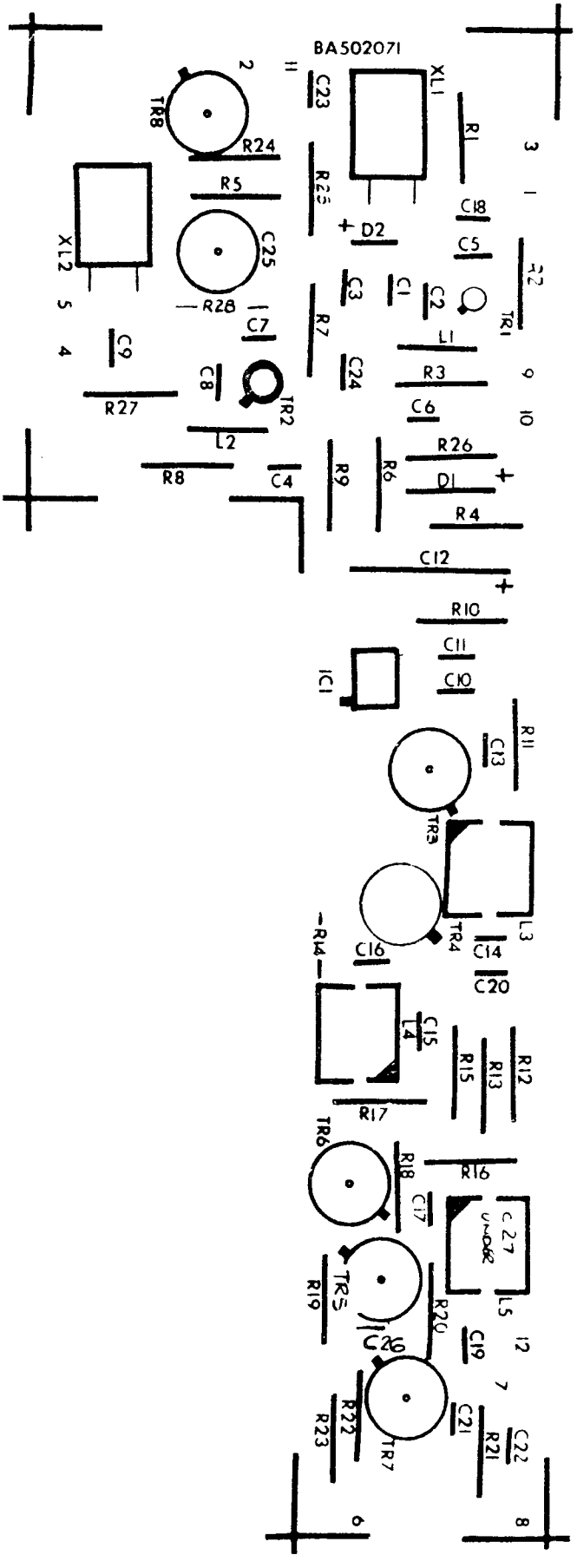
Component Layout: F.M./C.W. Detector Board Fig. 8



WOH8245/EC502186

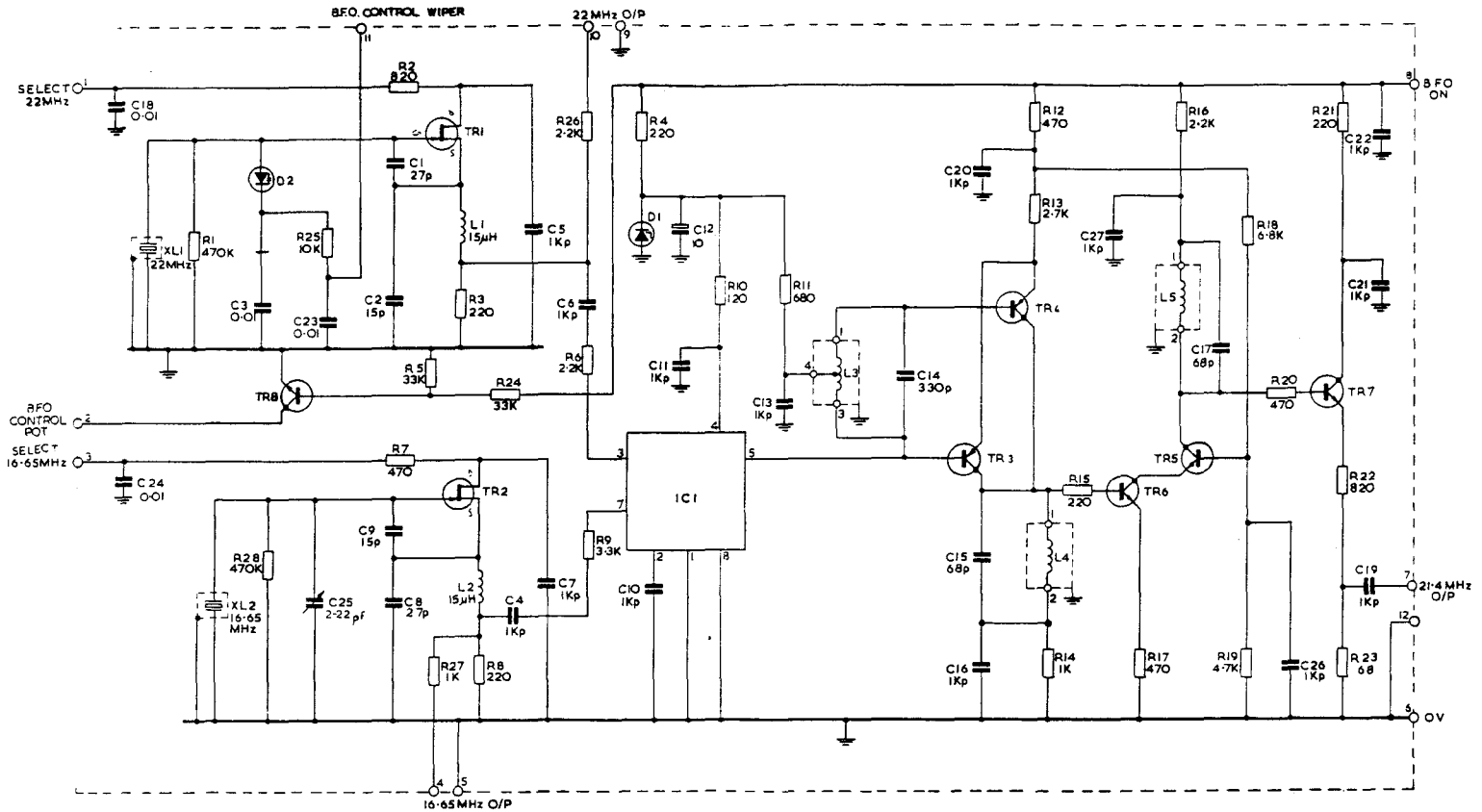
Circuit Diagram: F.M./C.W. Discrimination Board

Fig. 9



Component Layout: B.F.O. Board

Fig. 10



DIODES
D1 - BZY88C7V5
D2 - 88 109 YELLOW

TRANSISTORS

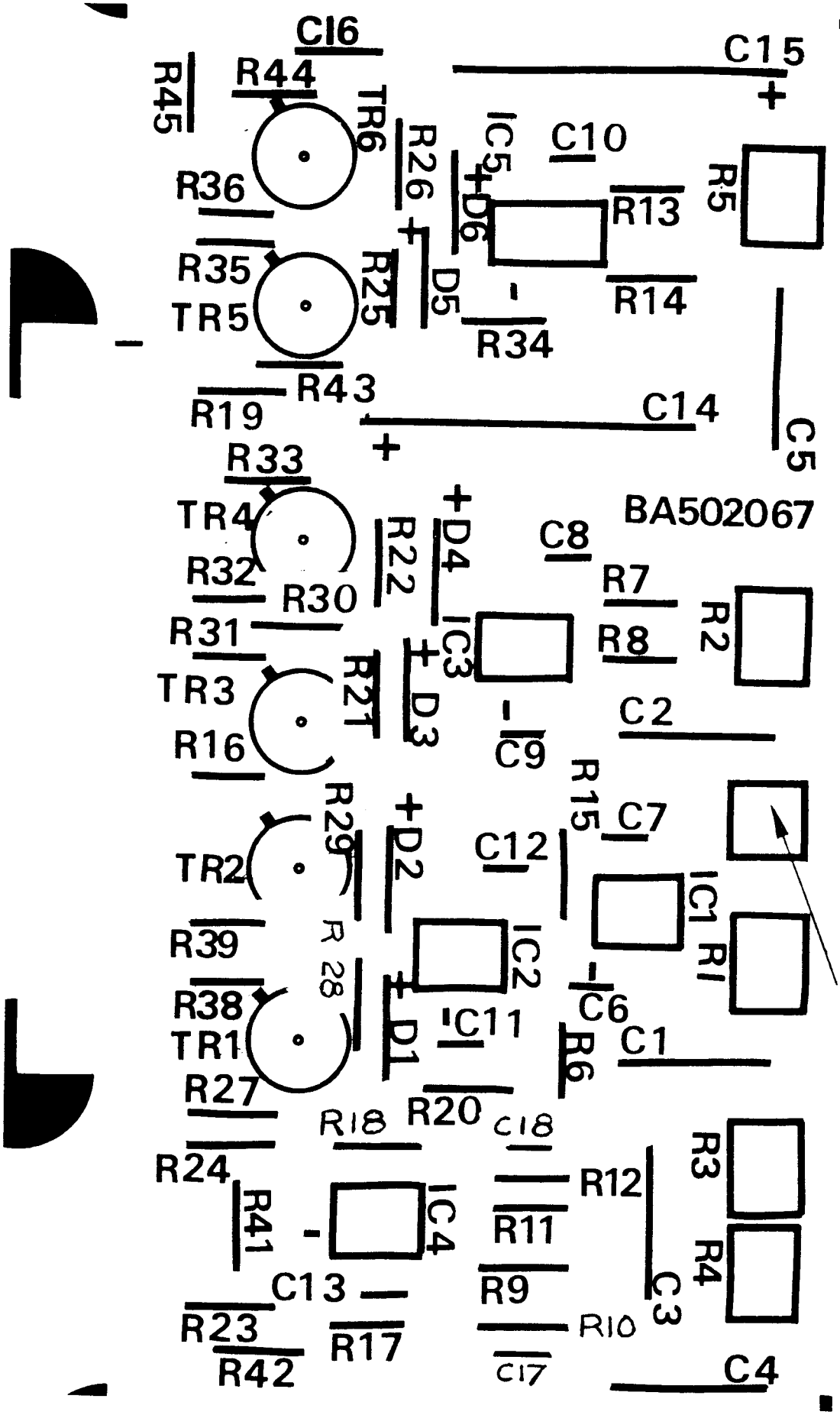
TR1	2N5397
TR2	2N4416
TR3,4,	BCY70
TR5,6,7,	2N2369
TR8	BC109

INTEGRATED CIRCUITS
IC1 SL641C

WOH 6245 | CC 502071
2

Circuit Diagram : B.F.O Board

Fig. 11



Component Layout: Video and Audio Amplifier Board

Fig. 12

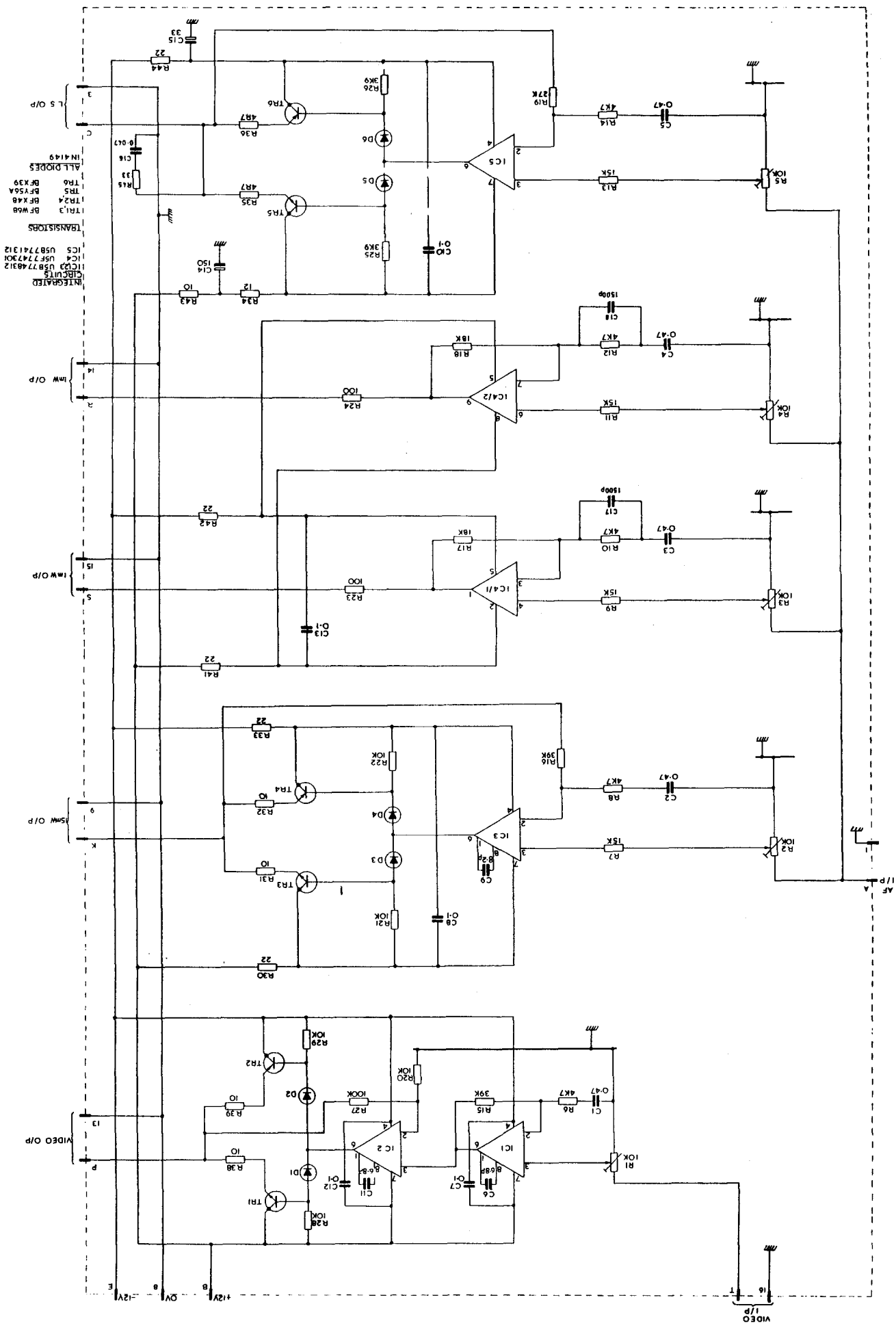
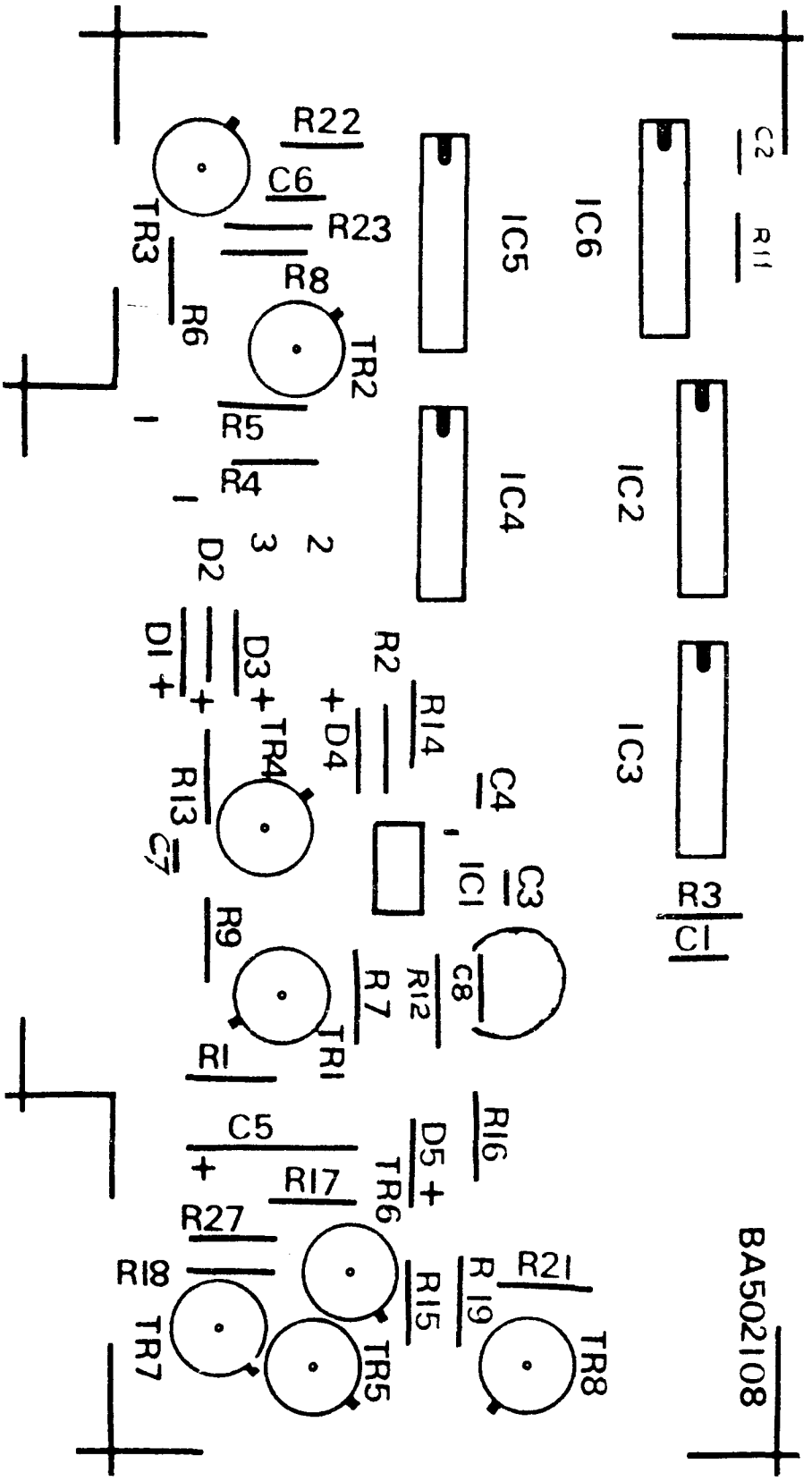


Fig.13

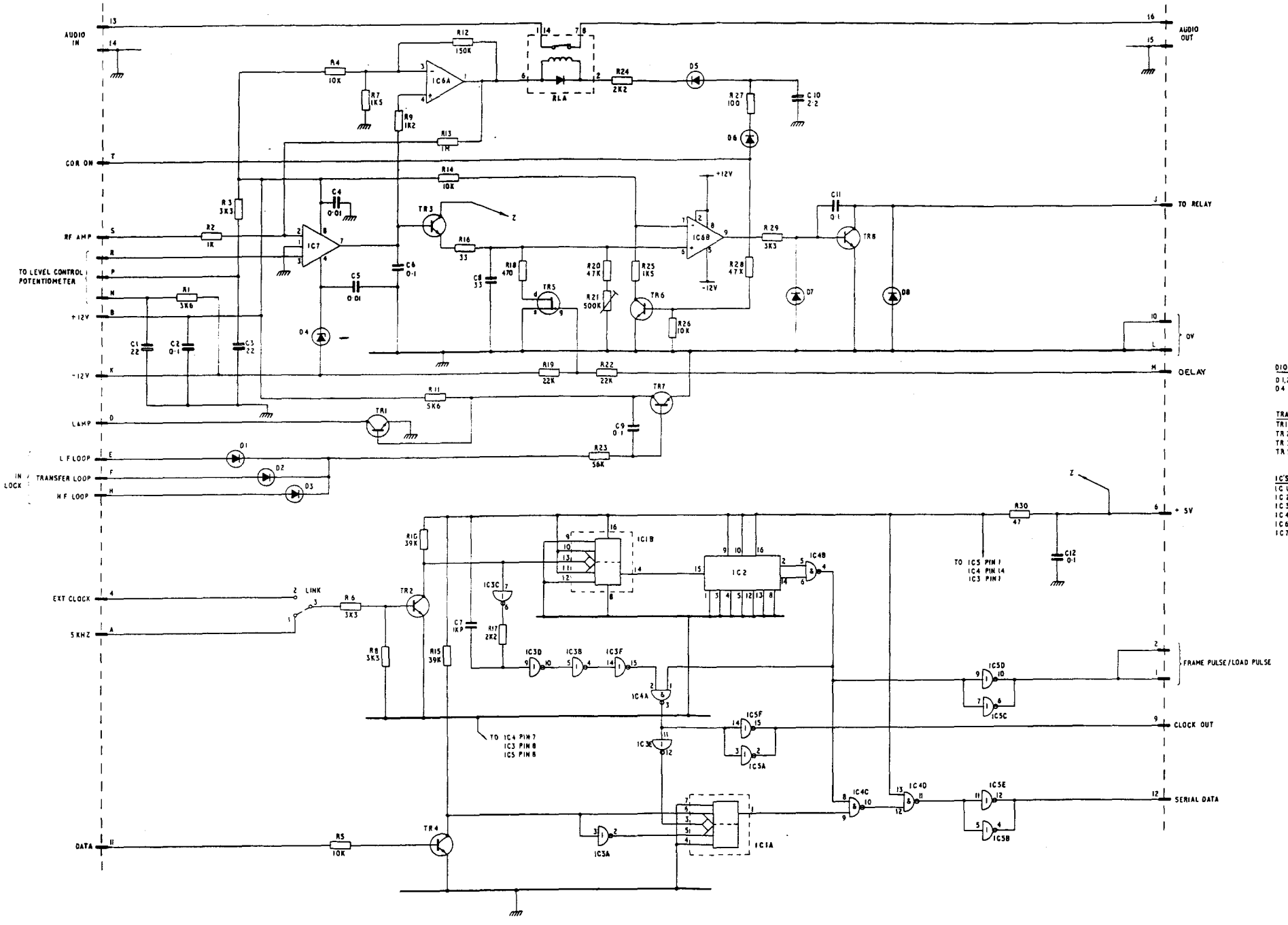
Circuit Diagram: Video and Audio Amplifier Board

WOH4215 DC502067 ST



Component Layout: C.O.R./SER. Control Board

Fig. 14



DIODES

D1,2,3,5,6,7,8.	IN 4149
D4	BZY88C6V2

TRANSISTORS

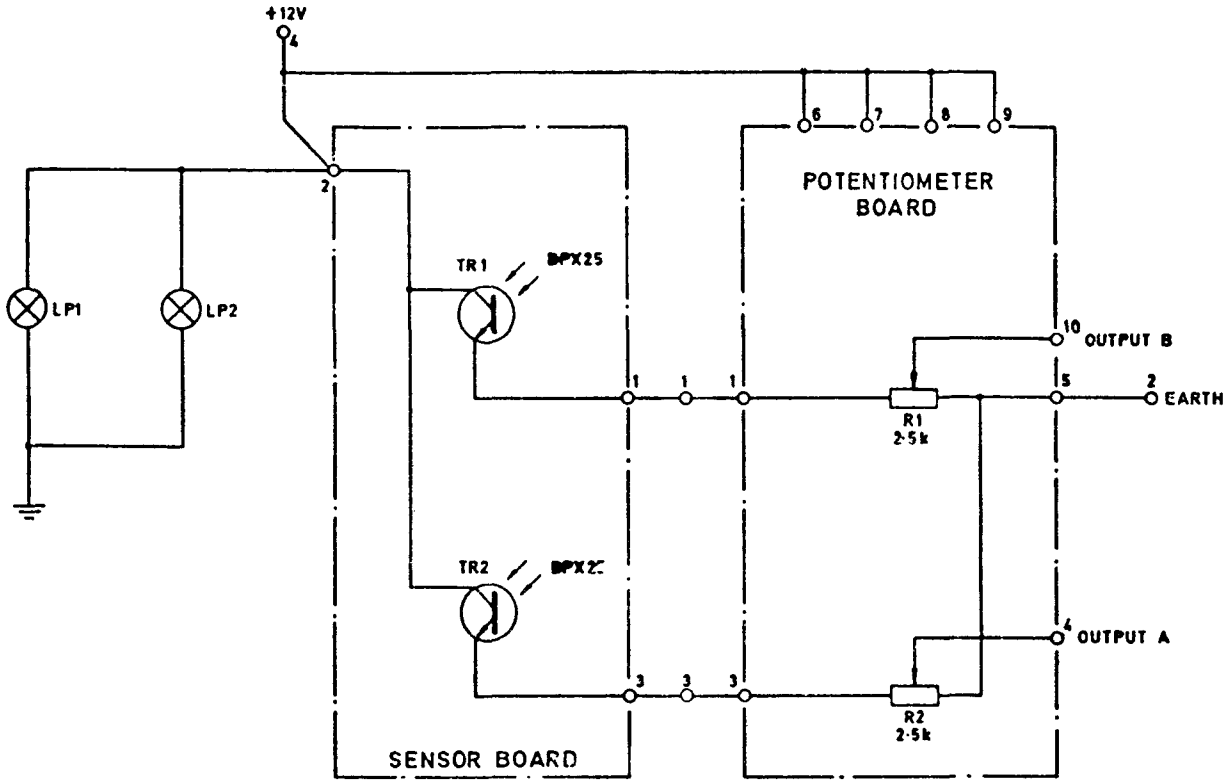
TR1,7,8.	BC 109
TR 2,4.	2N 2369
TR 3,6.	BC 107
TR 5	U 1897E

IC'S

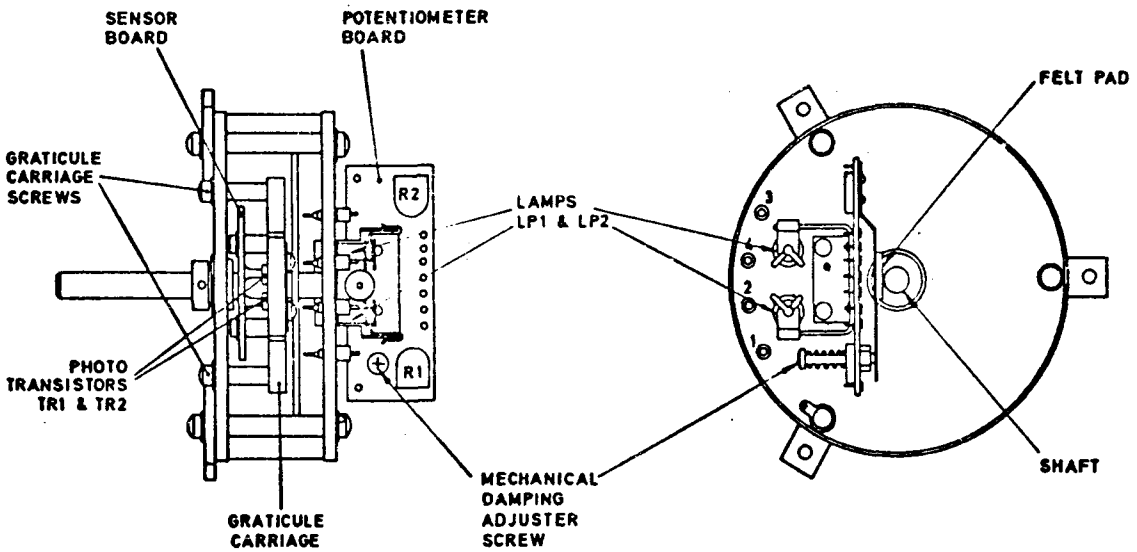
IC 1	CD 4027AE
IC 2	CD 4029AE
IC 3,5	CD 4049AE
IC 4	CD 4011AE
IC 6	CA 747T
IC 7	SN 52510L

WOH 6245 | 590057 SHT 2

Circuit Diagram : Cor/ Serialiser/Squelch Board Fig. 15

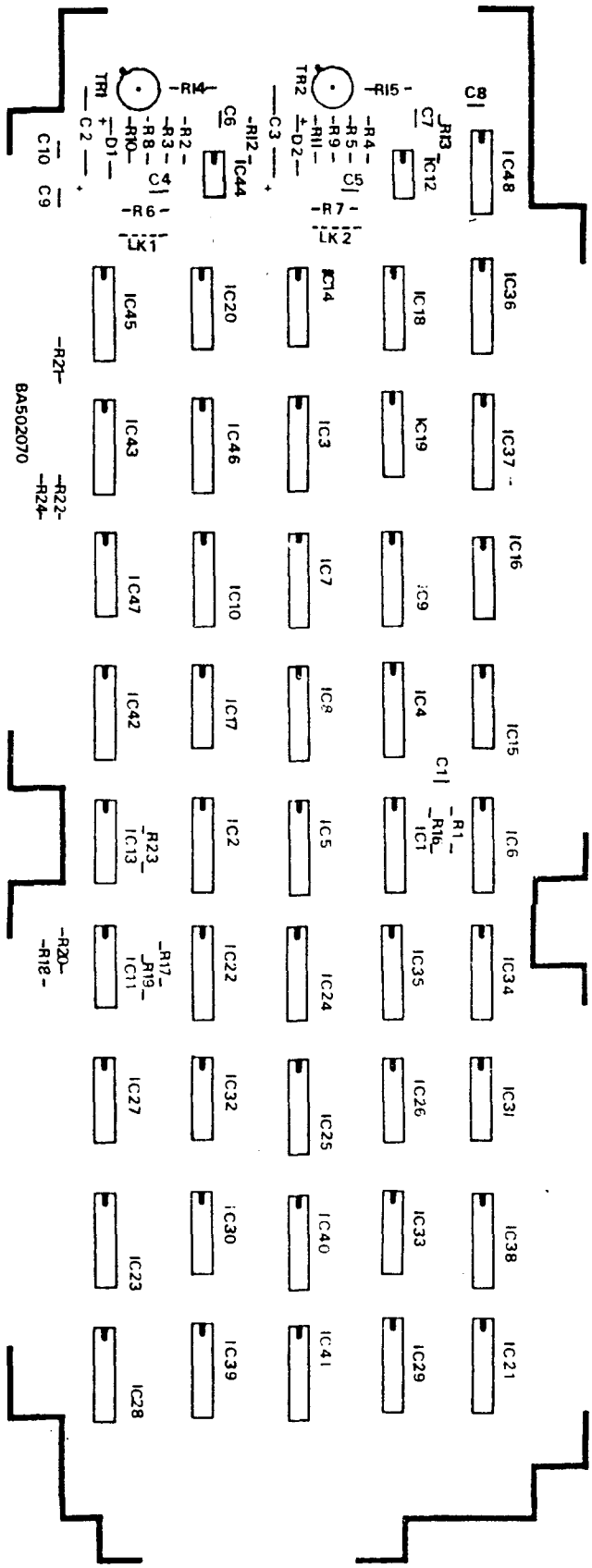


Circuit



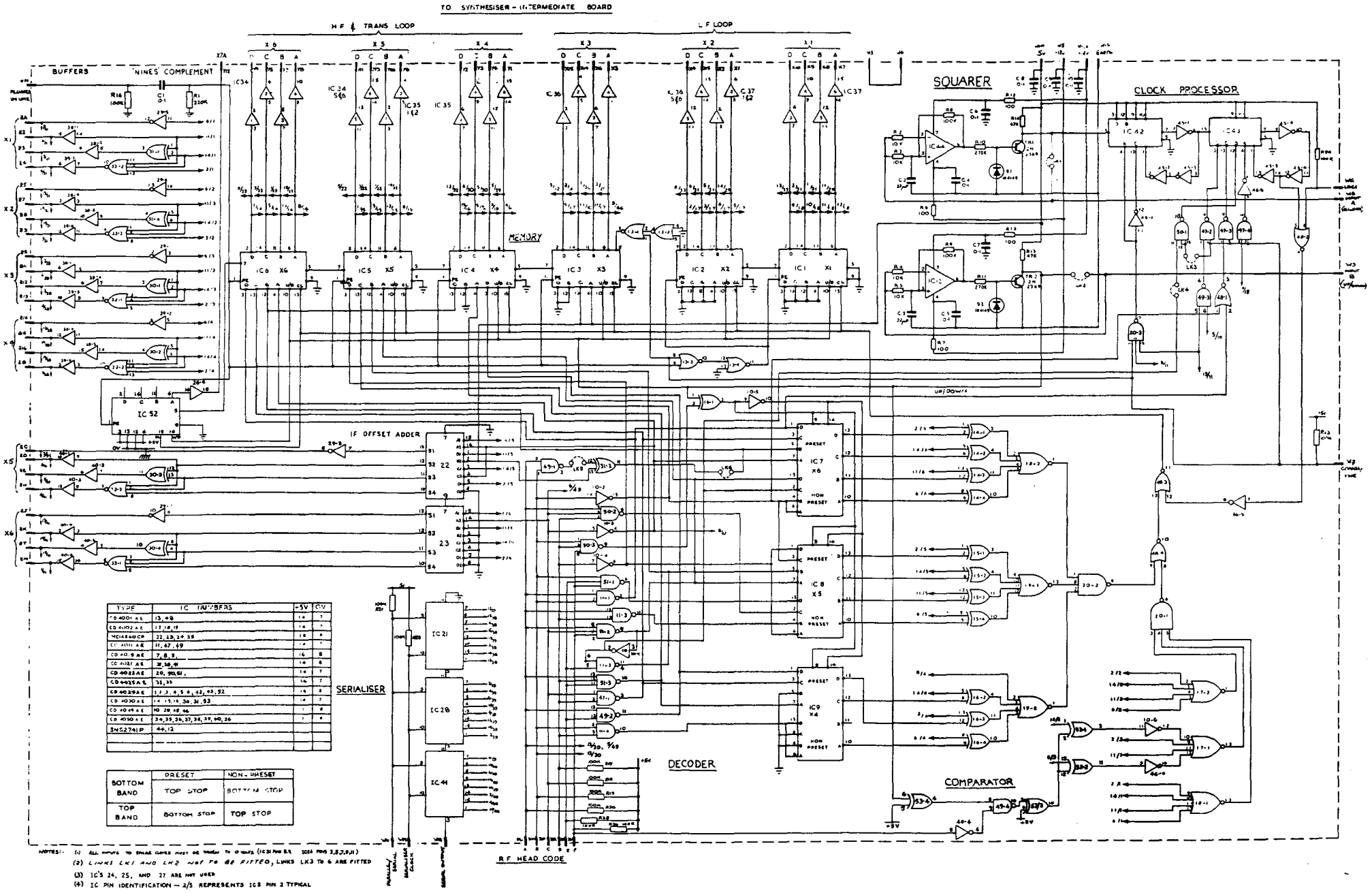
Layout

Component Layout and Circuit: Tuning Encoder Fig. 16



Component Layout: Logic Board

Fig. 17



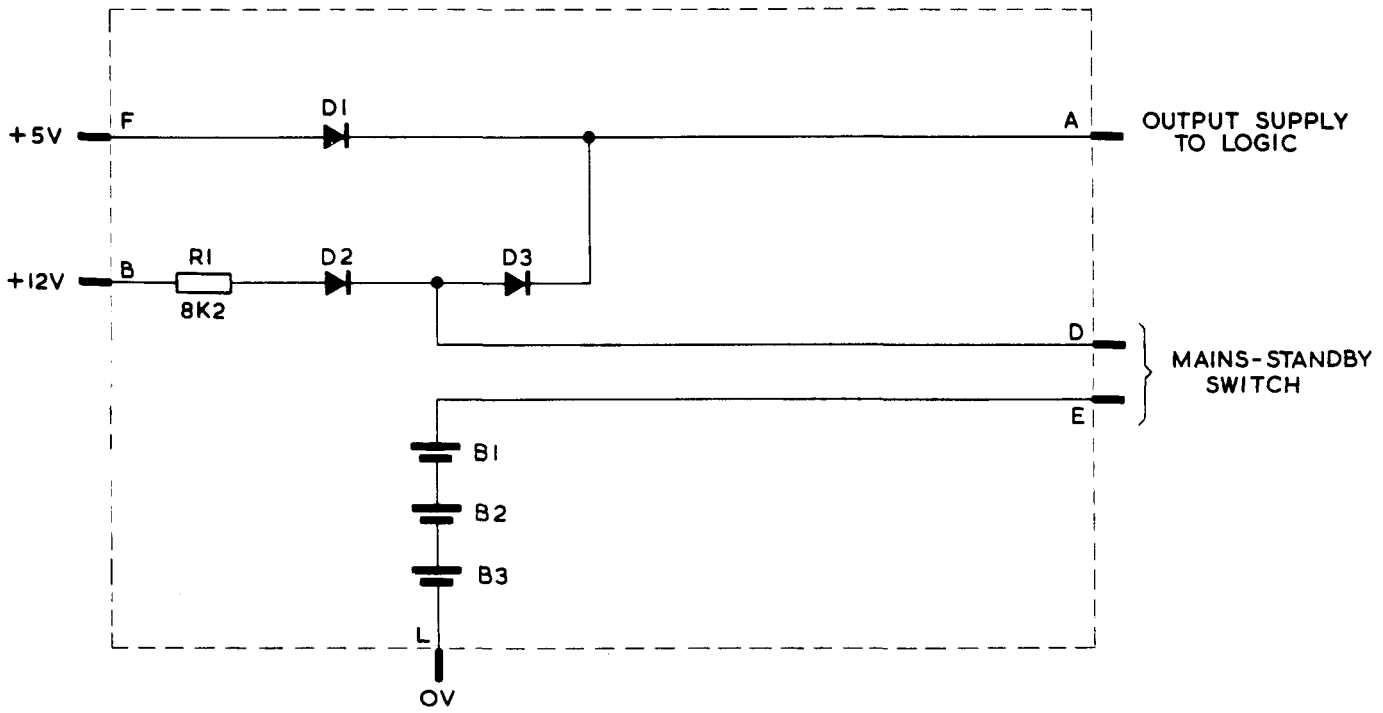
WDH 8245 59-0013, SHT 2

Circuit Diagram ; Logic Board

Fig.18

Component Layout: Battery Standby Supply

Fig. 19



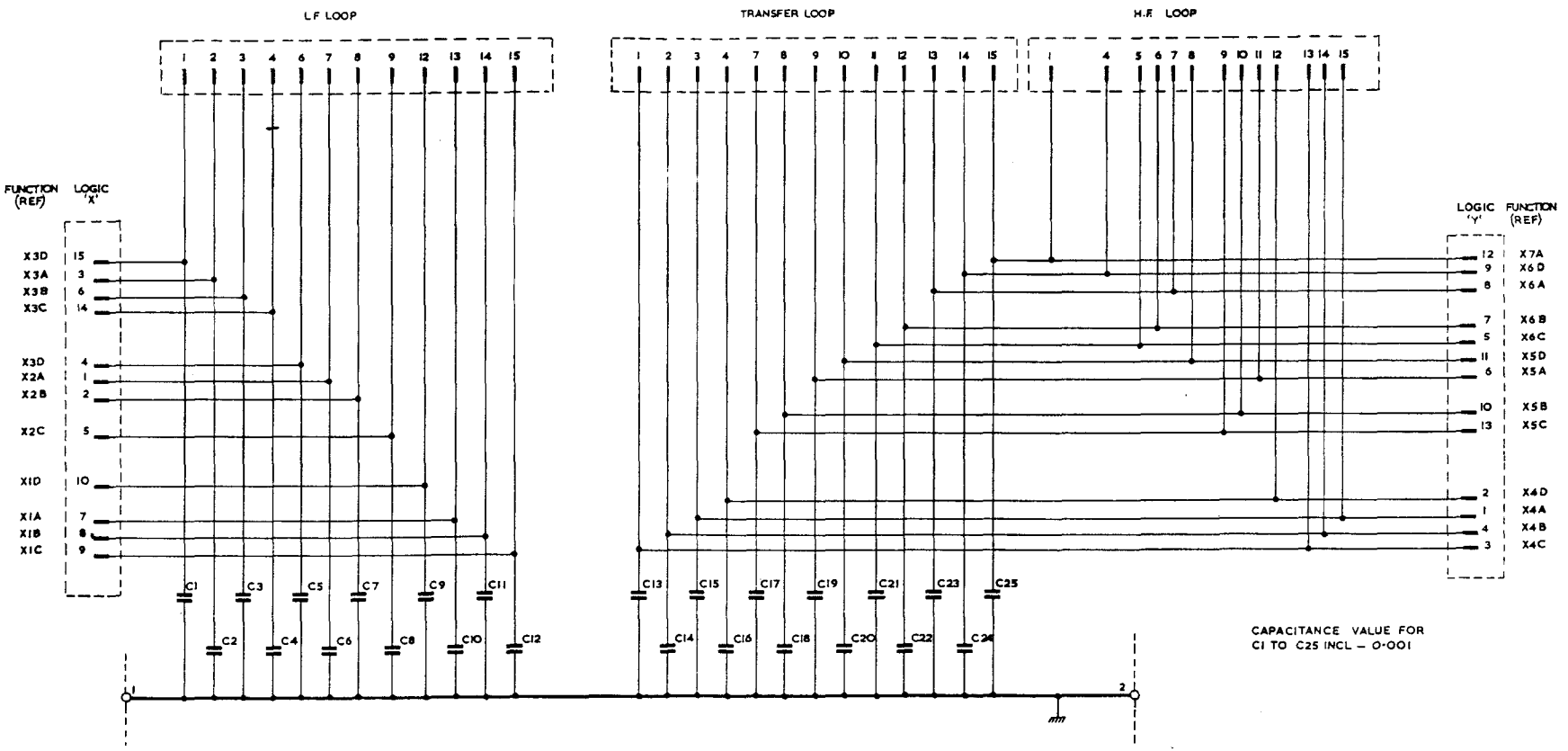
D1 & 2 IN4149
D3 OA47

Circuit Diagram: Battery Standby Supply

Fig. 20

Component Layout: Intermediate Logic Board

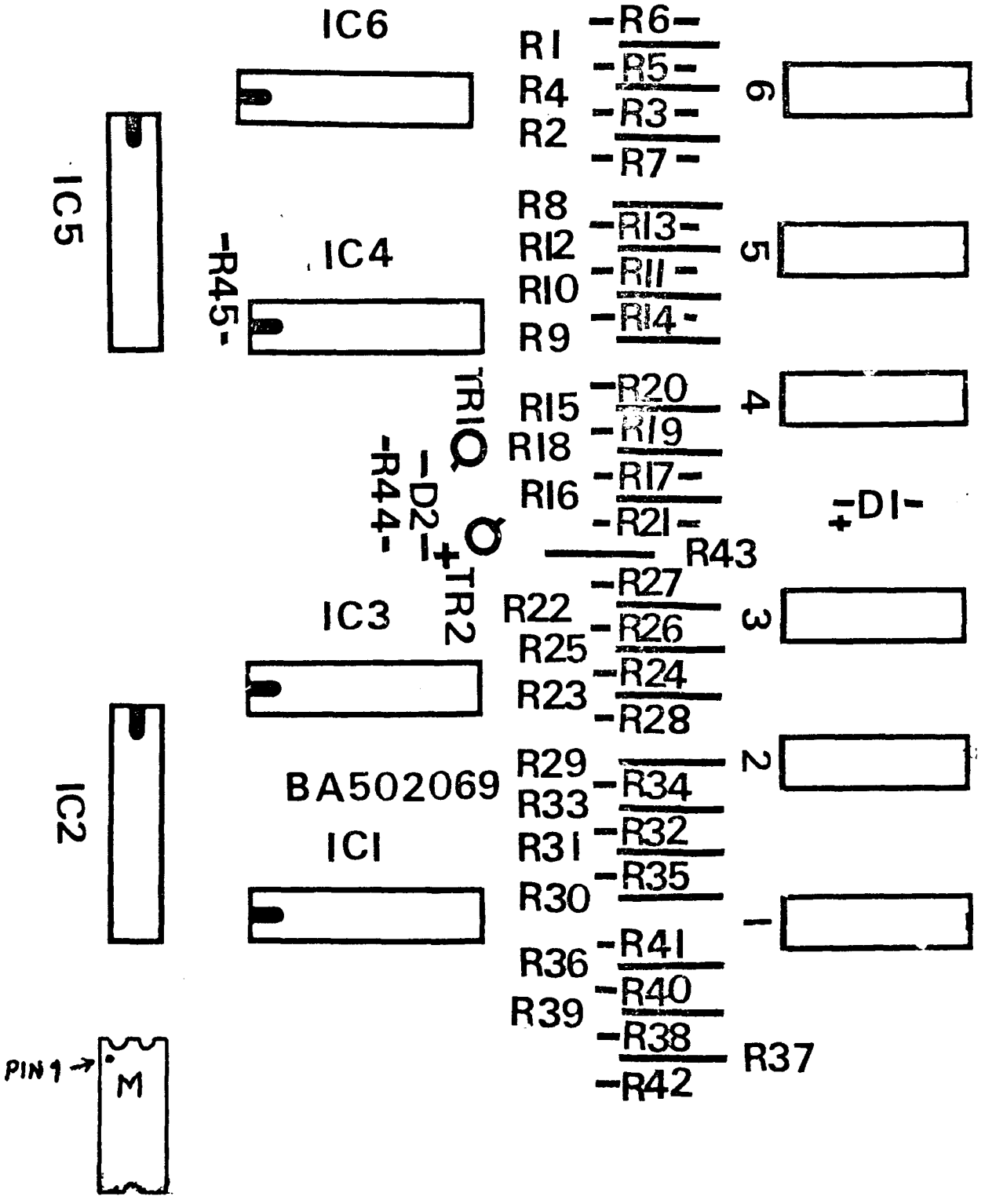
Fig. 21



WOH6245 | CC502068

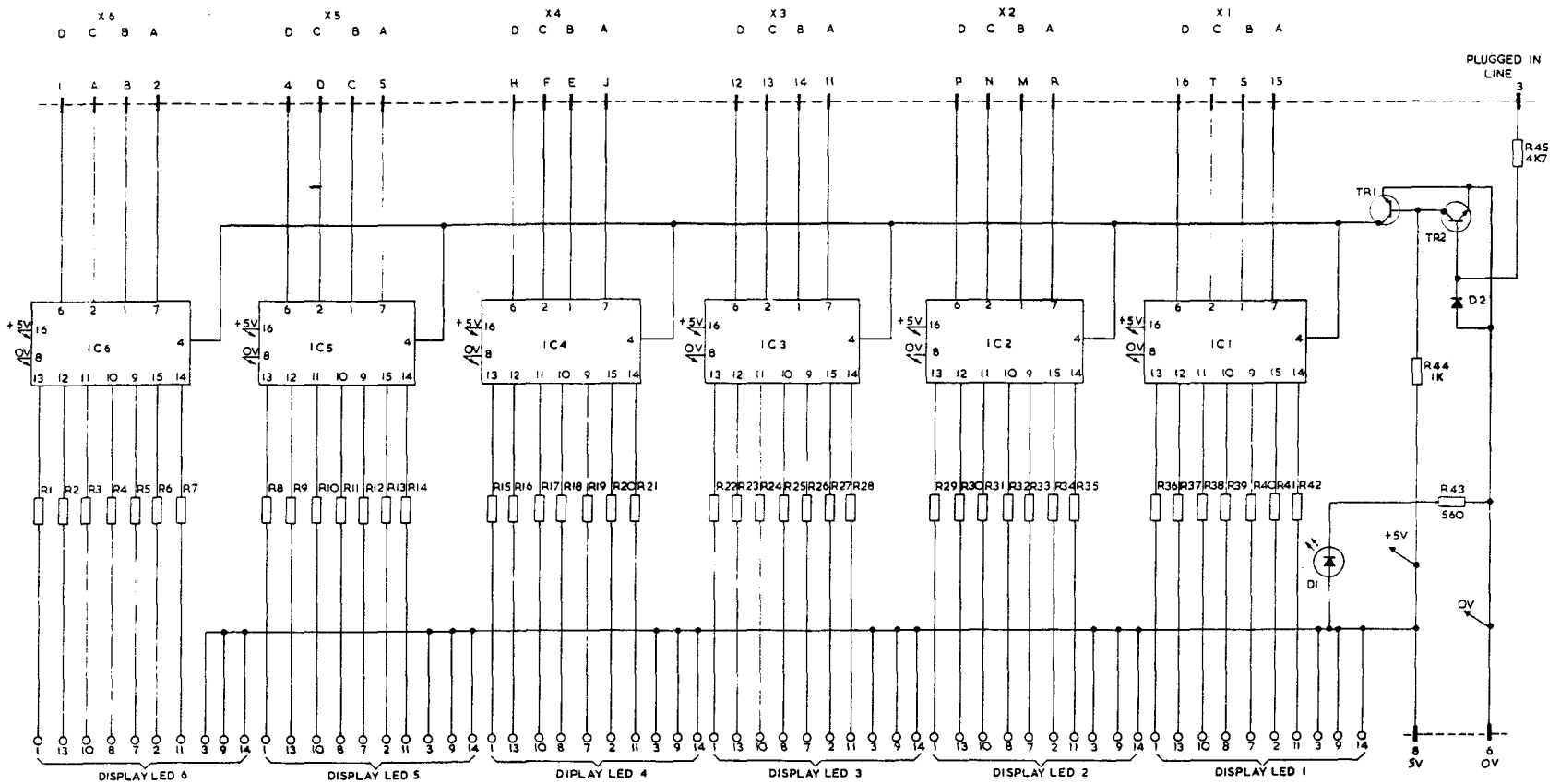
Circuit Diagram. Intermediate Logic Board

Fig.22



Component Layout: Frequency Display

Fig. 23



TRANSISTORS
TR1 & TR2 BC 109

IC'S
IC1-IC6 SN64L47N

DIODES
D1 MV50A
D2 IN4149

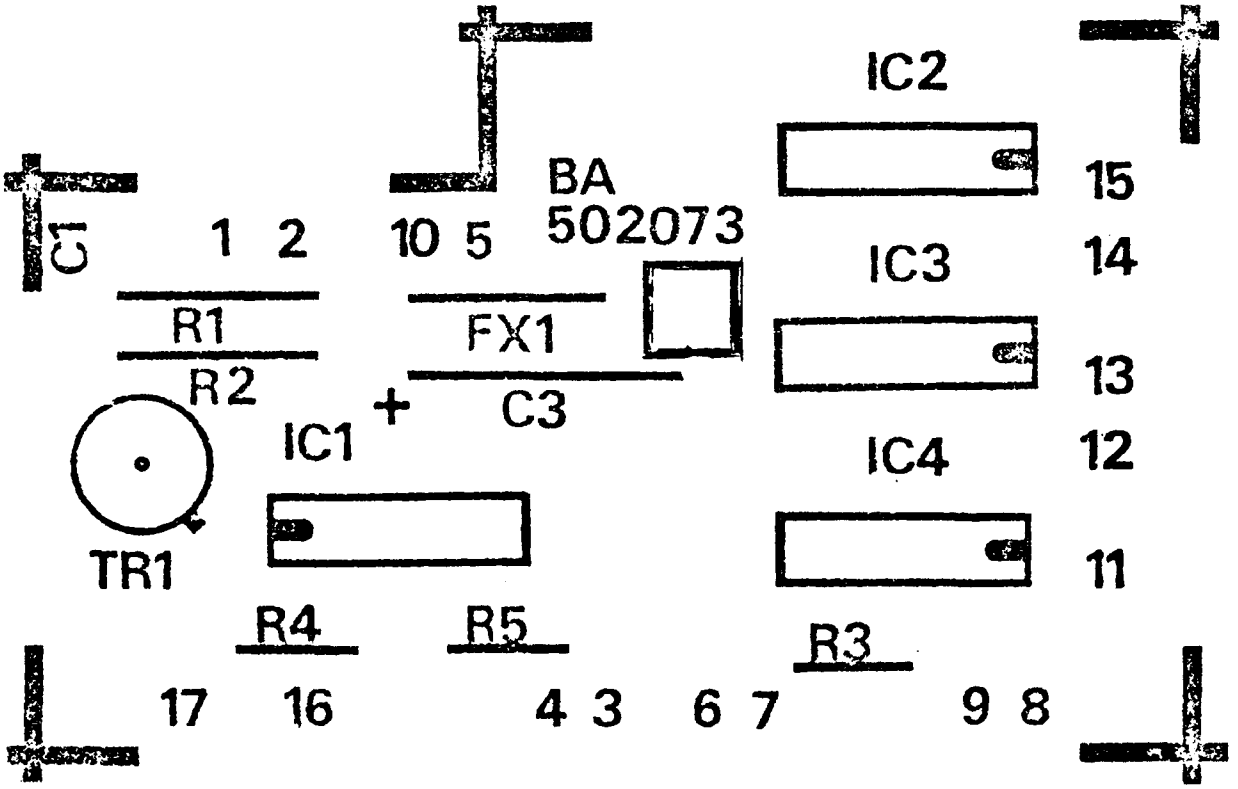
LED 1-6 MAN 10A

R1-42 220 Ω

WOH 6245 CC502069
4

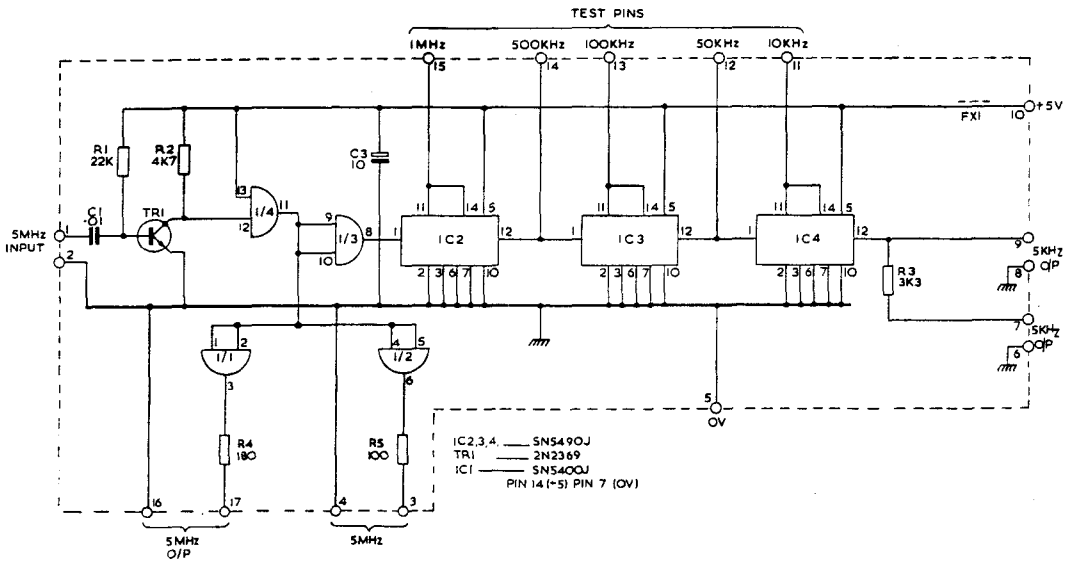
Circuit Diagram ; Frequency Display

Fig. 24



Component Layout: Divider Board

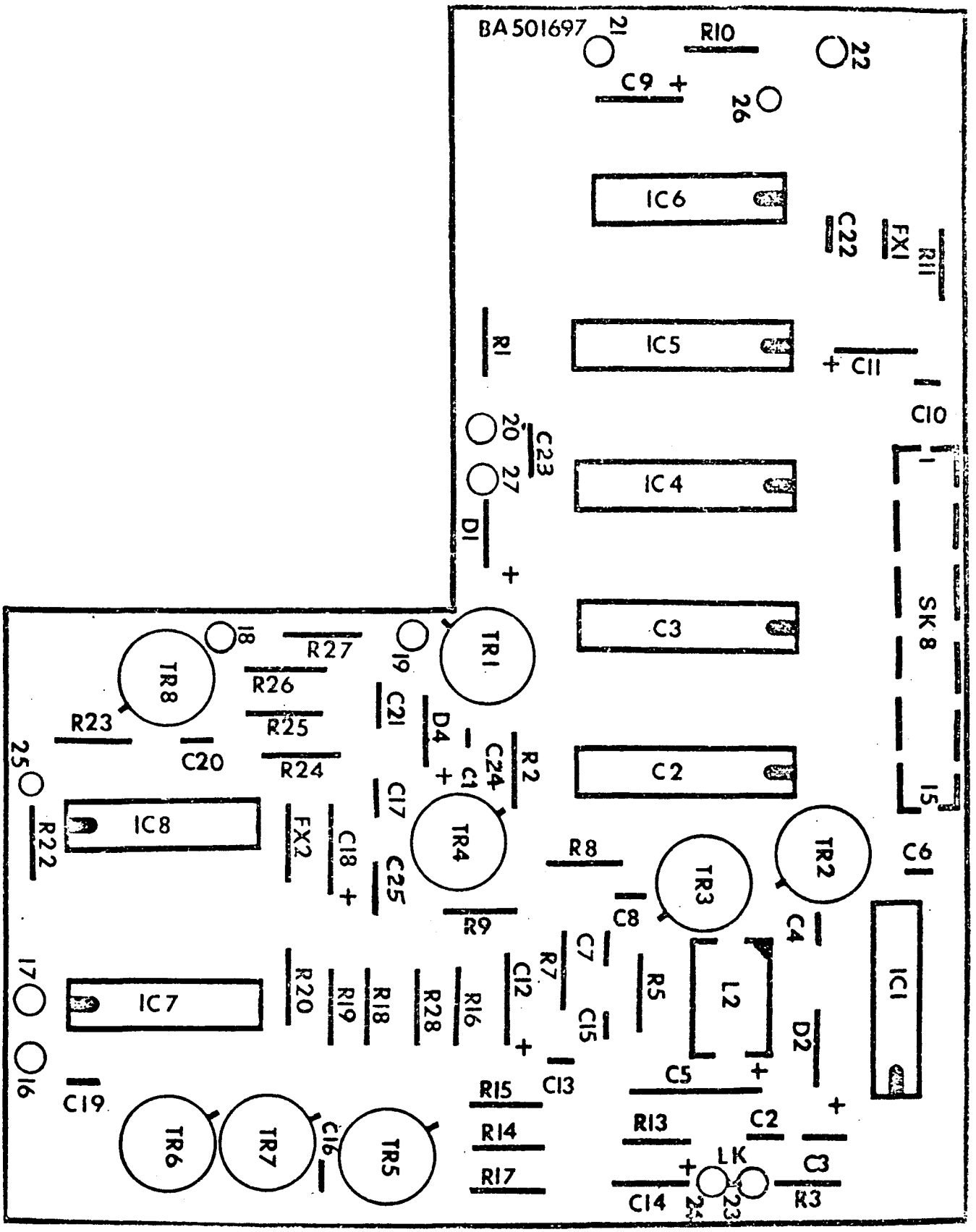
Fig. 25



WOH 6245 | BC502076
3

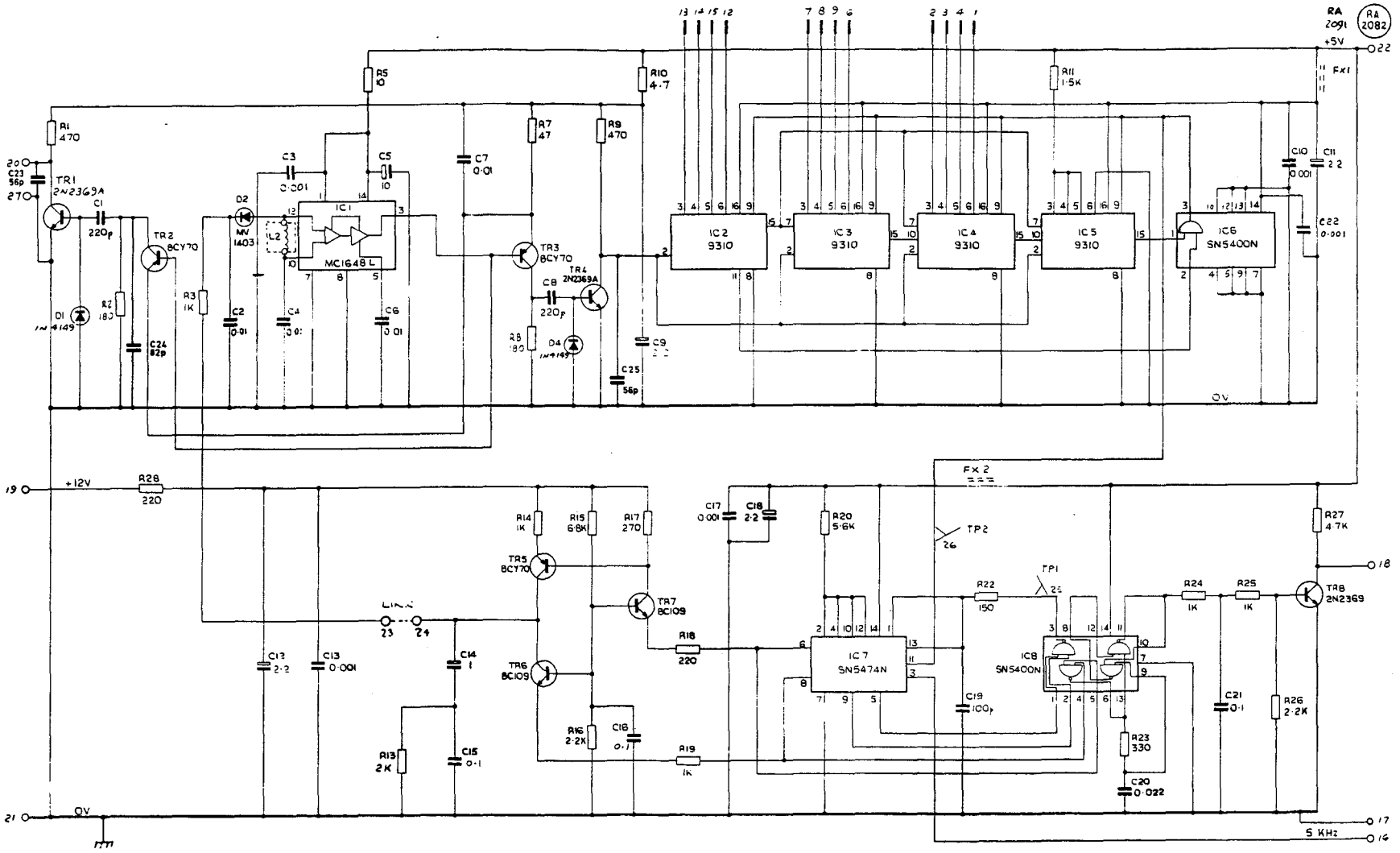
Circuit Diagram ; Divider Board

Fig. 26



Component Layout: L.F. Loop

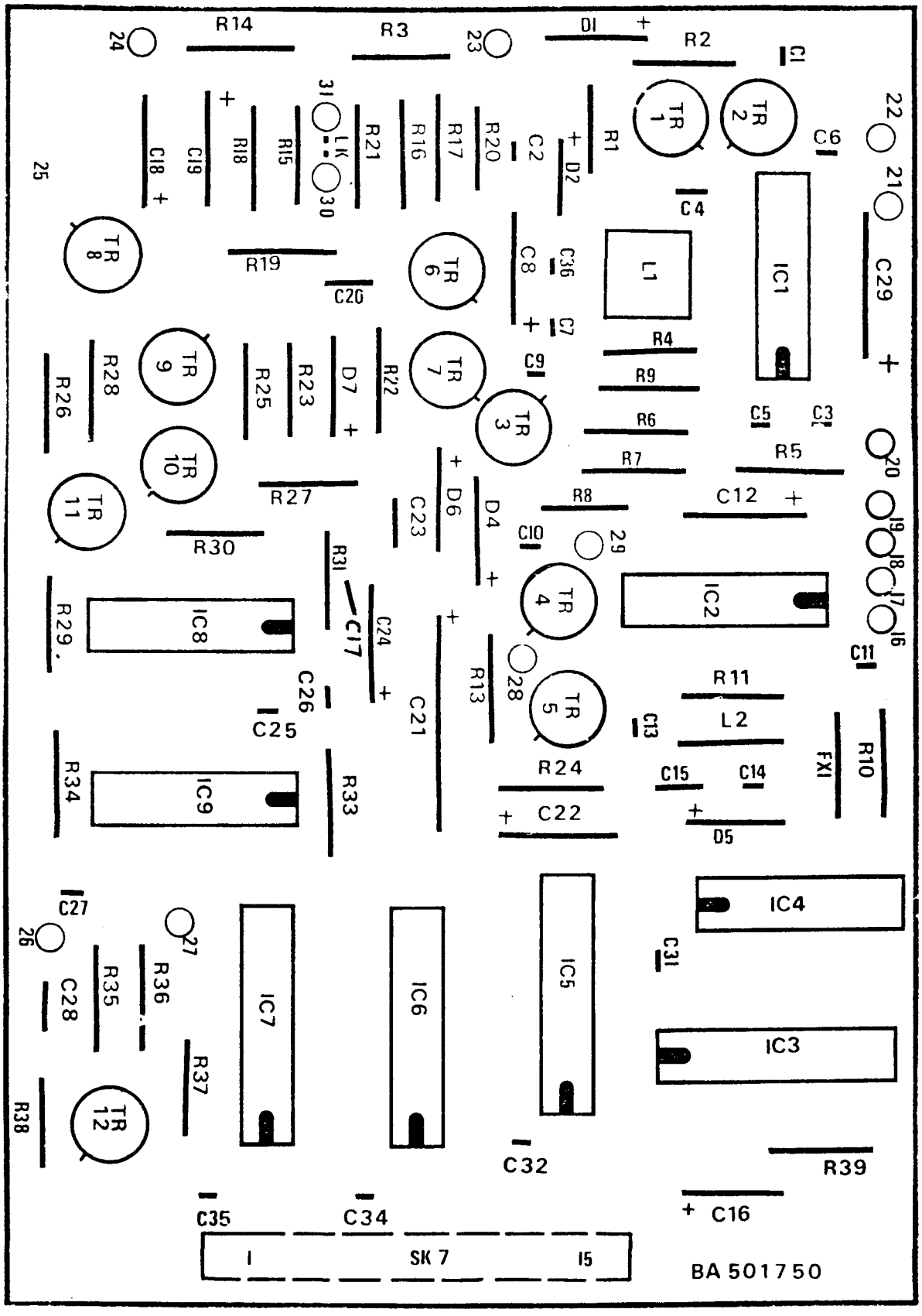
Fig. 27



WOH6245 | CC501697

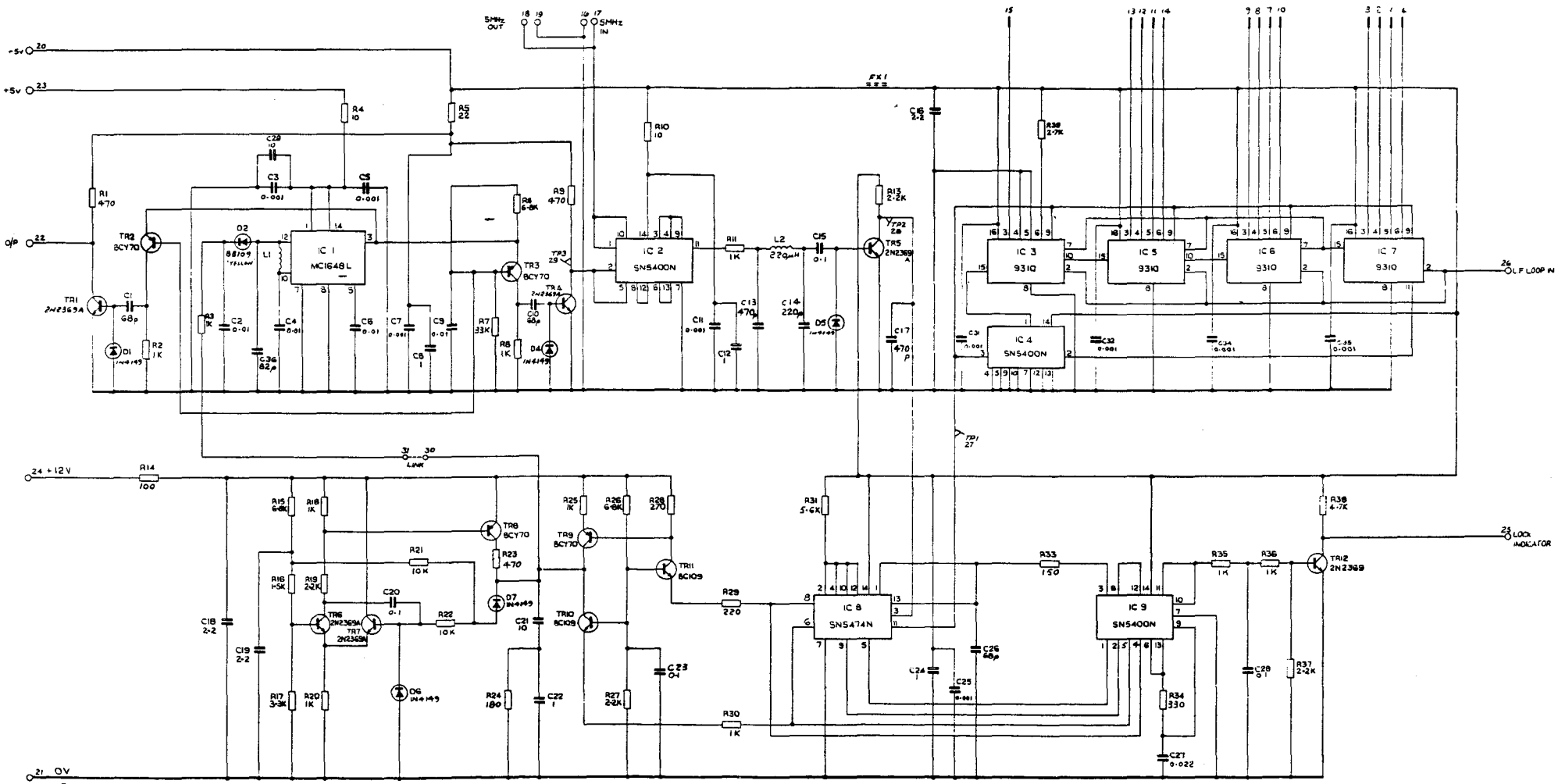
Circuit Diagram: L.F. Loop

Fig. 28



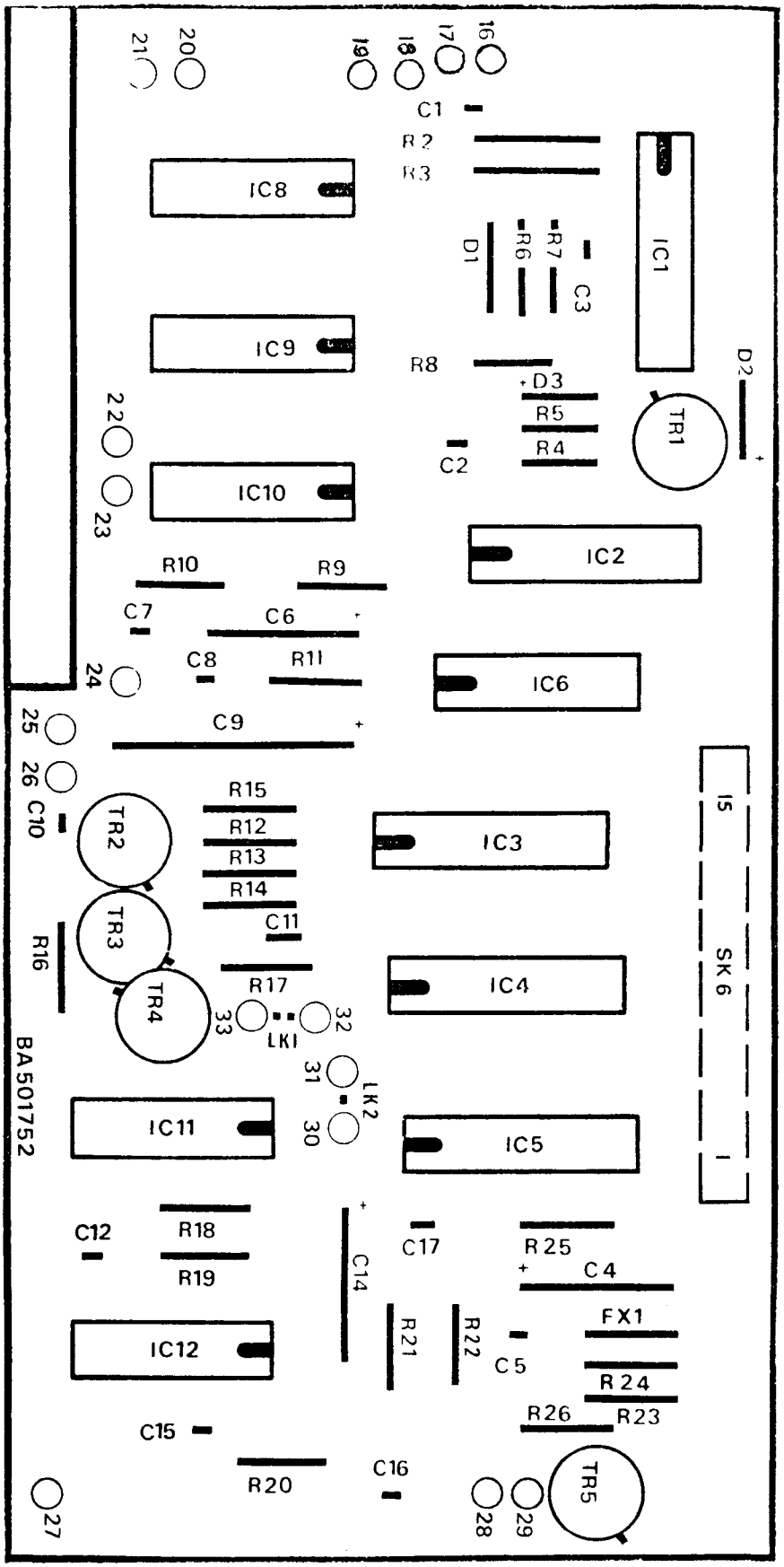
Component Layout: Transfer Loop

Fig. 29



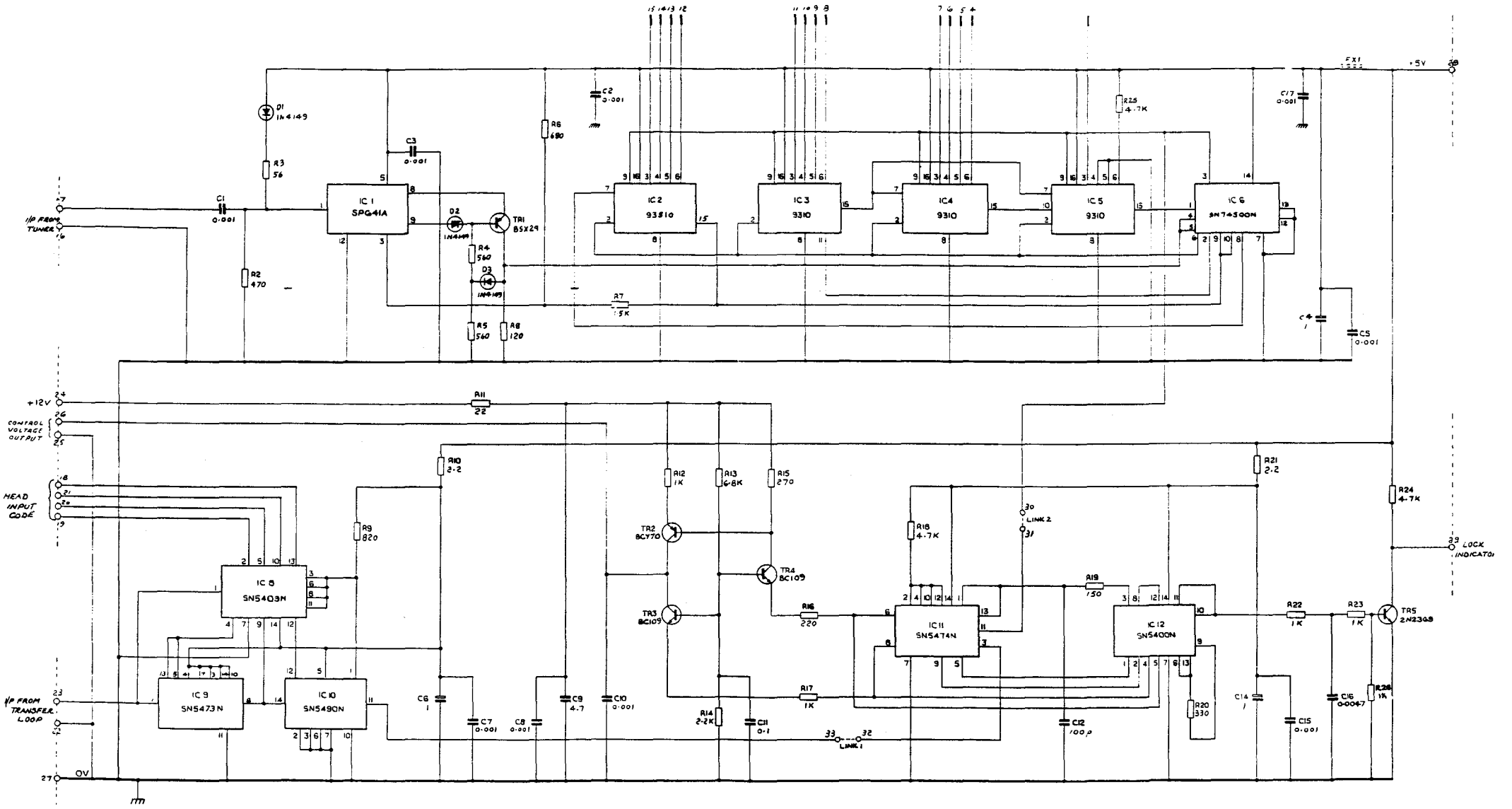
Circuit Diagram: Transfer Loop

Fig. 30



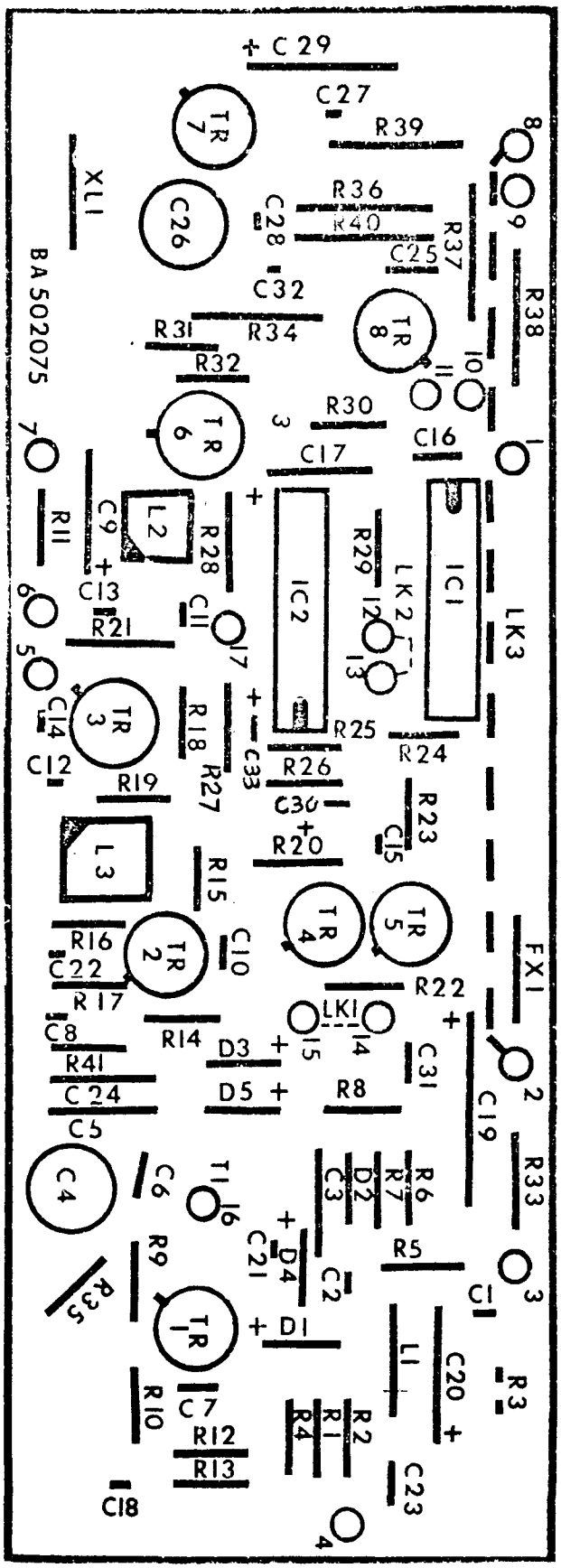
Component Layout: H.F. Loop

Fig. 31



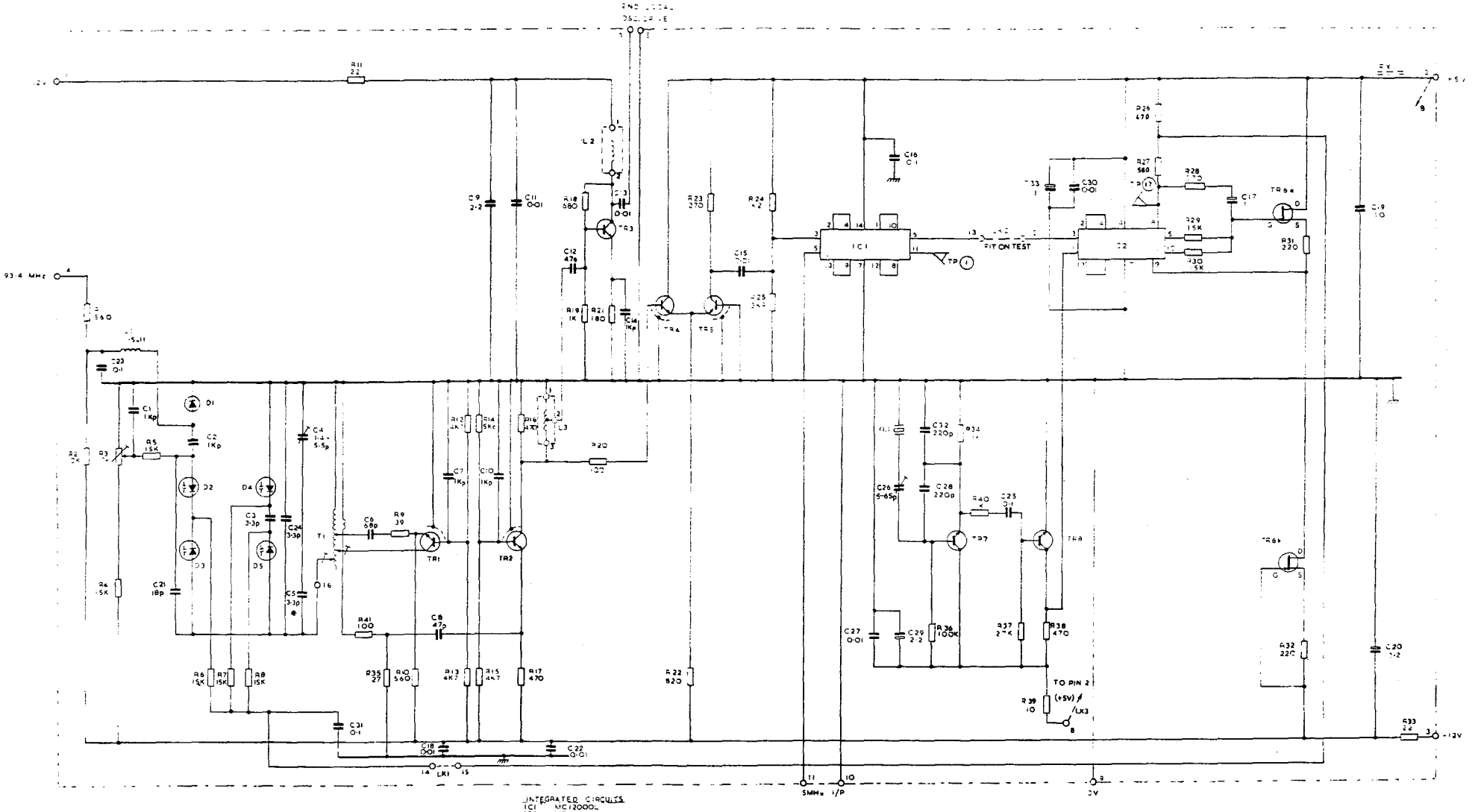
Circuit Diagram : H.F. Loop

Fig.32



Component Layout: 2nd Local Oscillator

Fig. 33



* CAPACITOR C5 MAY BE REPLACED WITH A WIRE LINK ON TEST

INTEGRATED CIRCUITS
IC1 MC12000L
IC2 MC4344L

TRANSISTORS
TR2 & 5 2N918 TR1 2N3571
TR3 BFR34
TR6 U235
TR7 BC109
TR8 2N2369A

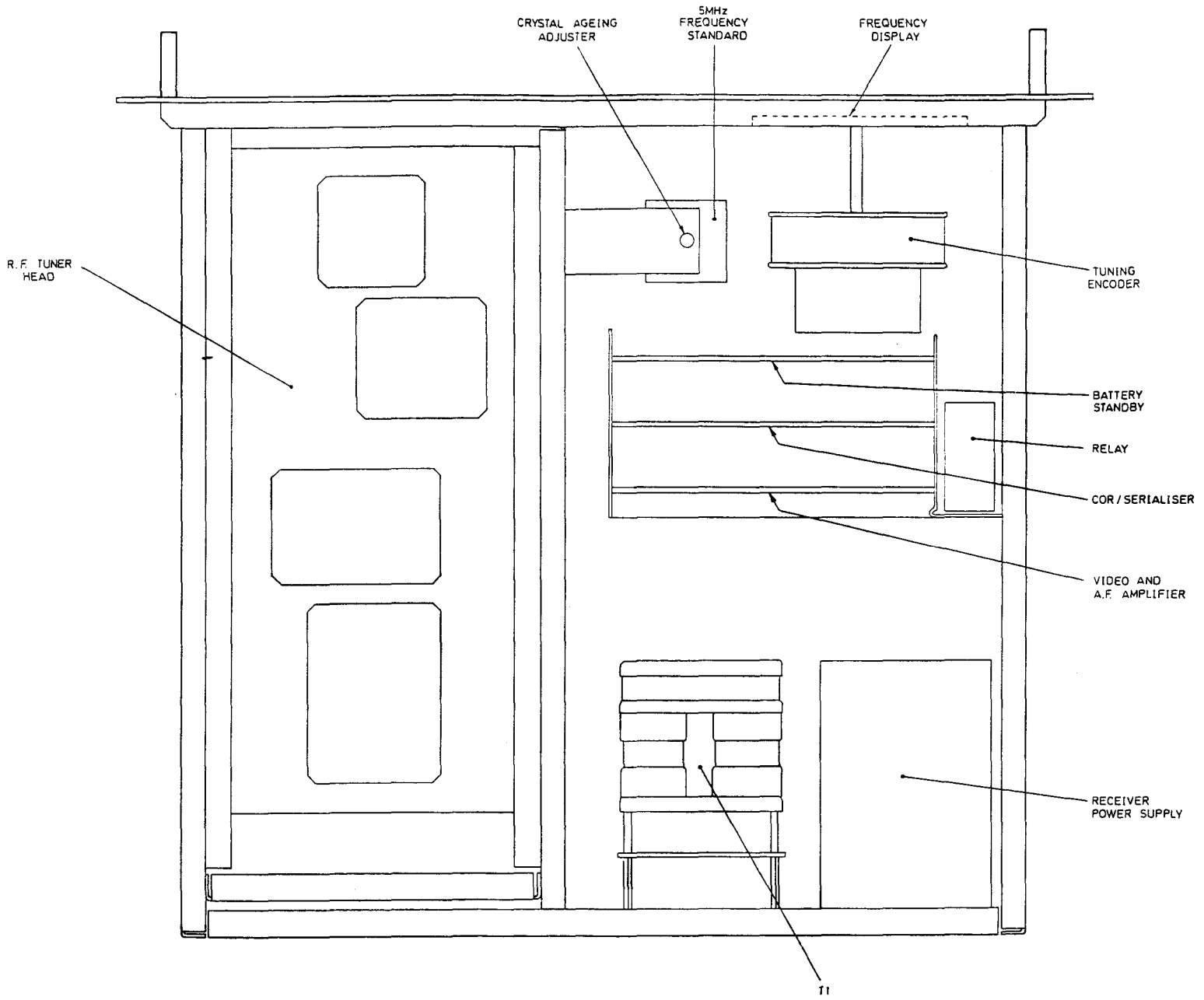
DIODES
D1, MPN 3401
D2,3 BB109 "YELLOW"
D4,5 BB105B

NOTE TRANSFORMER T1 IS INCORPORATED IN THE TRACKING ON THE BOARD

WDH6245 | DC502075 | 8

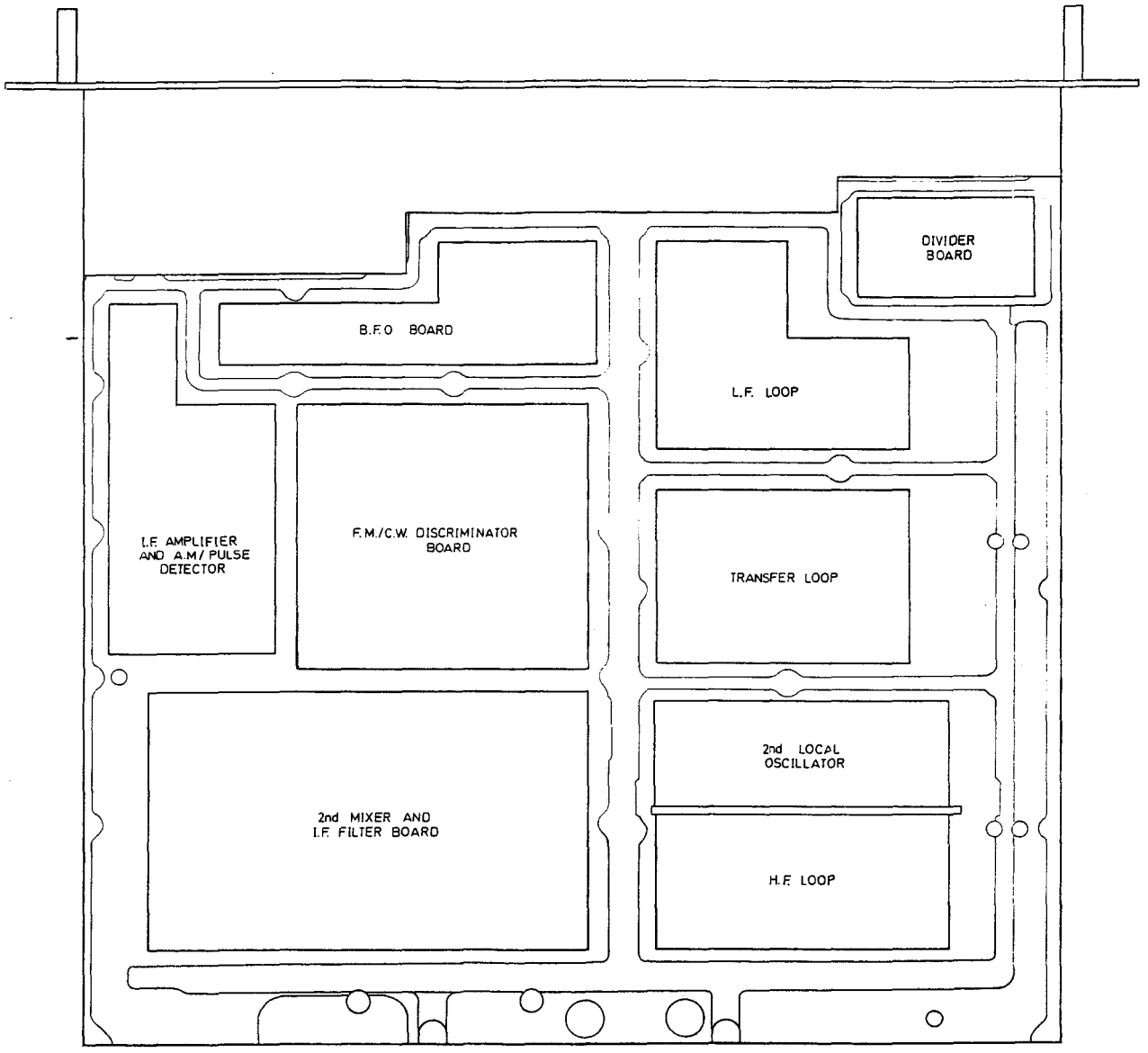
Circuit Diagram ; 2nd Local Oscillator

Fig.34



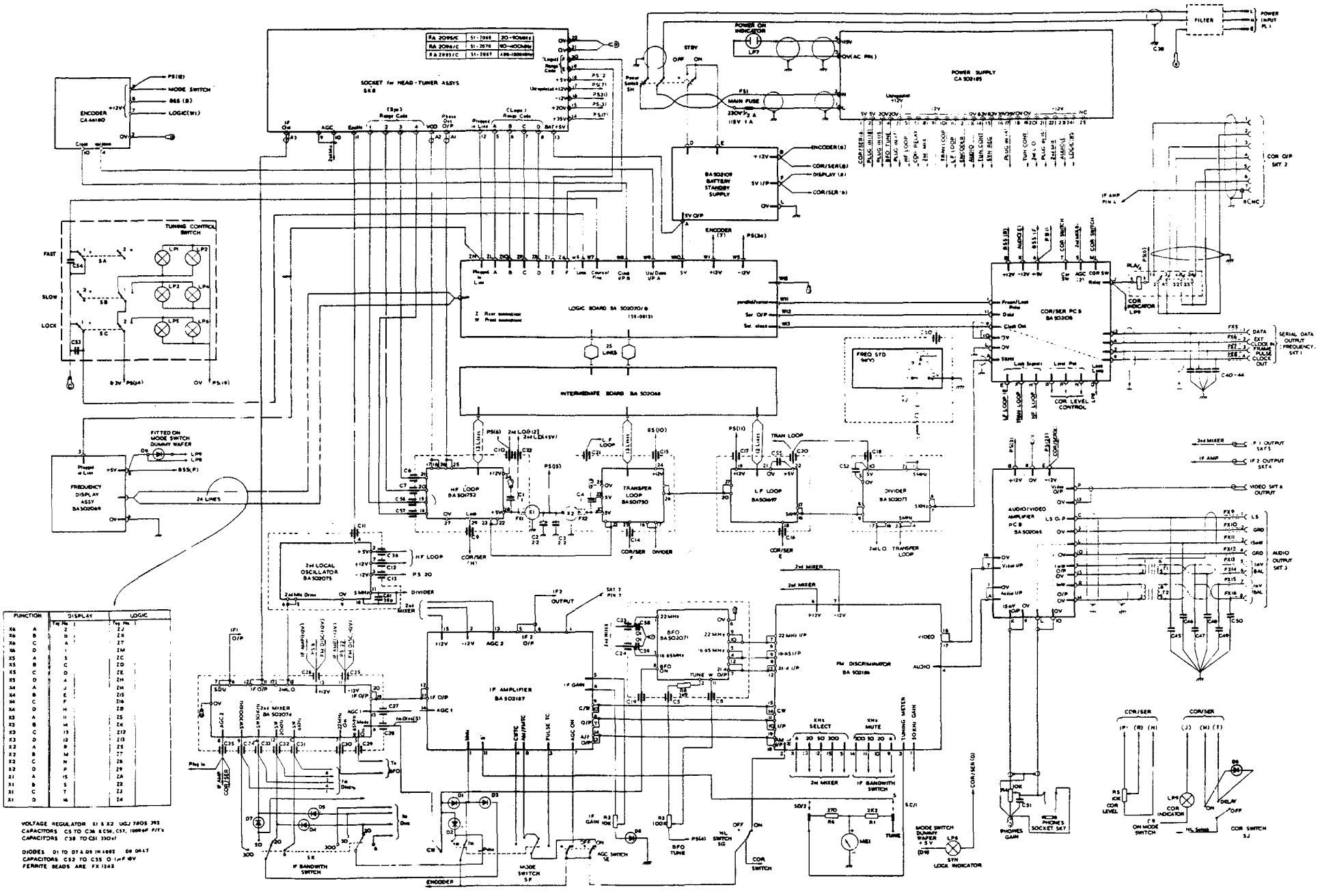
Chassis Top: RA.2091C Receiver Unit

Fig.35



Chassis Underside: RA.2091C Receiver Unit

Fig. 36



FUNCTION	DISPLAY		LOGIC	
	Tag No.		Tag No.	
X6 A	2		Z J	
X6 B	9		Z K	
X6 C	A		Z T	
X6 D	I		Z M	
X5 A	S		Z C	
X5 B	C		Z D	
X5 C	F		Z E	
X5 D	A		Z H	
X4 A	J		Z N	
X4 B	E		Z 15	
X4 C	K		Z 16	
X4 D	H		Z B	
X3 A	11		Z 5	
X3 B	M		Z K	
X3 C	13		Z 12	
X3 D	12		Z 13	
X2 A	B		Z 5	
X2 B	M		Z 7	
X2 C	N		Z 8	
X2 D	P		Z 9	
X1 A	15		Z A	
X1 B	S		Z 2	
X1 C	T		Z 3	
X1 D	16		Z 4	

VOLTAGE REGULATOR X1 & X2 UCJ 78D5 393
CAPACITORS C5 TO C36 & C50, C57, 1000pF F/T's
CAPACITORS C38 TO C51 330nF
DIODES D1 TO D7 & D9 IN 4002 D8 OA47
CAPACITORS C52 TO C55 0.1mF 40V
FERRITE BEADS ARE FX 1242

Interconnection Diagram: RA 2091C Receiver

Fig 37